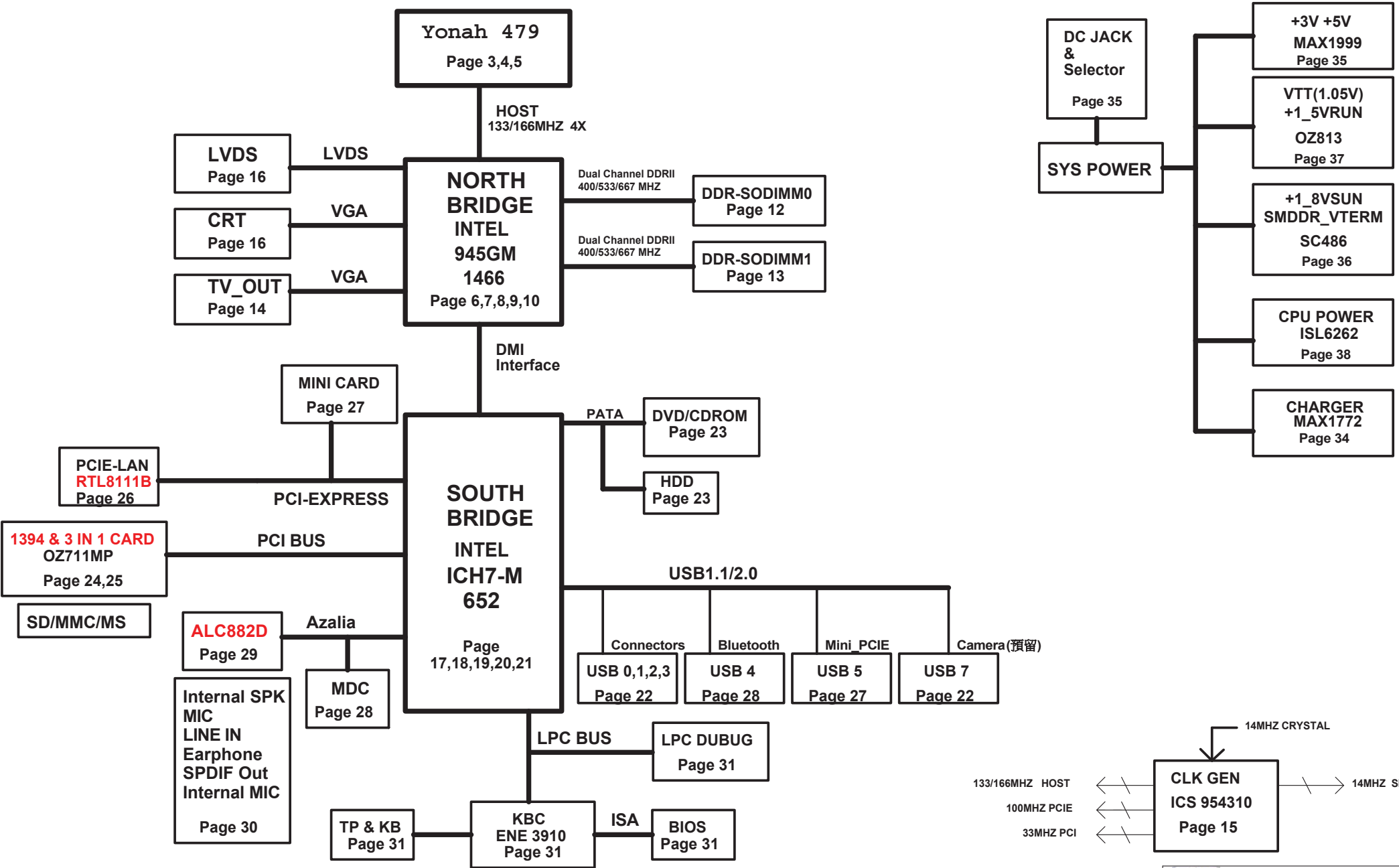


MS1034 VER:0.A



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Voltage Rails




Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHCORE	Core Voltage for Processor	VR_ON
VTT	1.05 rail for Processor & 945GM I/O	RUN_ON
+1_5VRUN	1.5V switched power rail(off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND
SMDDR_VTERM	0.9V DDRII Termination voltage (off in S4-S5)	DIMM_ON
+1_8VSUS	1.8V power rail DDRII (off in S4-S5)	DIMM_ON
+2_5VRUN	2.5V power rail for 945GM LVDS	+3VRUN
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

Voltage	Description	Control Signal
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	+5VSUS

 GND	DIGTIAL GROUD	
 AGND	AUDIO GND	
	POWER Analogy GND	

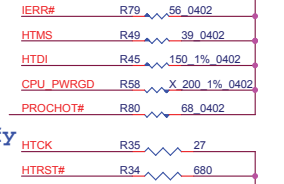
PCI RESOURCE

DEVICE	IDSEL#	REQ/GNT#	PCI_INT#	CLOCK
SOUTHBRIDGE	AD31(INT)	NA	NA	PCLK_CARD
CARDREADER	AD20	0	A	

6 HA#[3..31] <<> HA#[3..31]
6 RS#[0..2] >> RS#[0..2]
6 HREQ#[0..4] <<> HREQ#[0..4]
6 HASTB#[0..1] <<> HASTB#[0..1]

6 HD#[0..63] <<> HD#[0..63]
6 HDSTBP#[0..3] <<> HDSTBP#[0..3]
6 HDSTBN#[0..3] <<> HDSTBN#[0..3]
6 DBI#[0..3] <<> DBI#[0..3]

VTT=1_05V

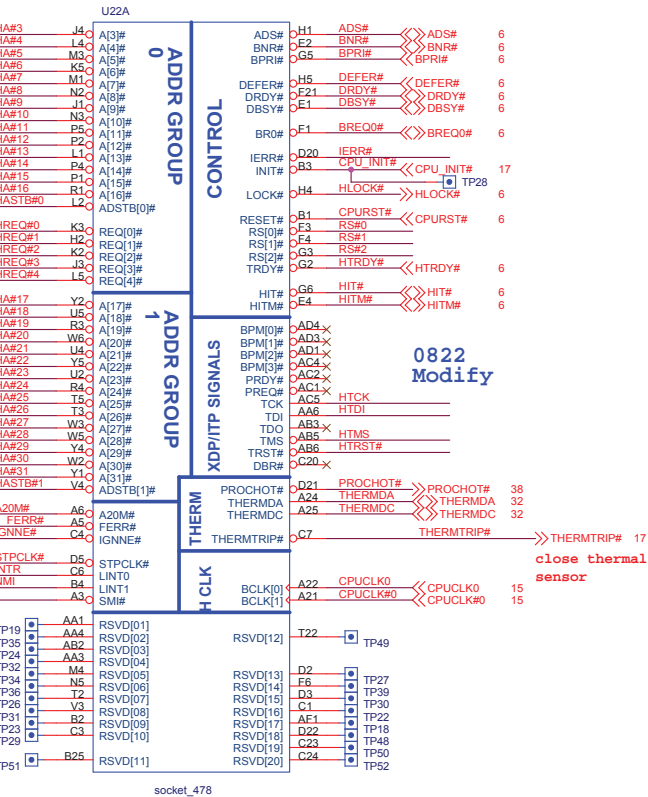
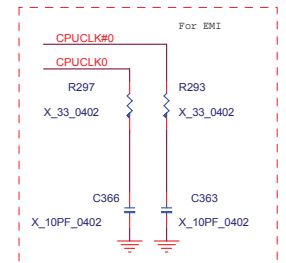


0822
Modify

Reserve : CPU_PWRGD
CPU_PWRGD :
Demo board no EPU

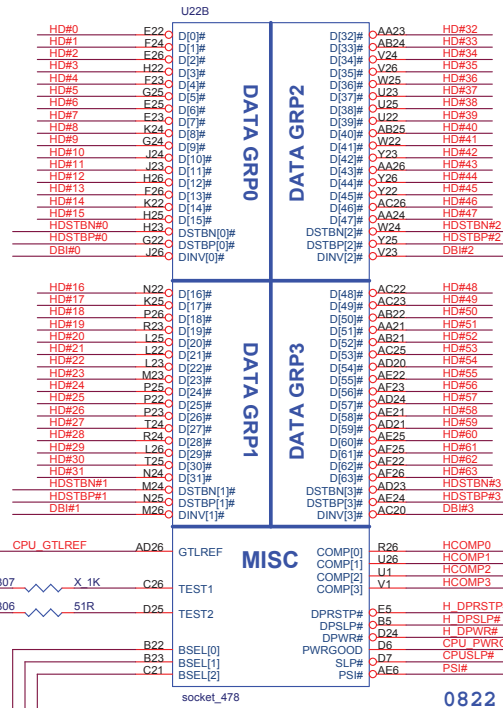
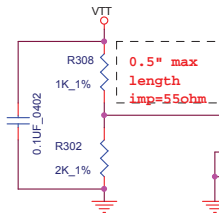
0.5" max length
25 MIL AWAY FROM HIGH
SPEED SIGNAL
HCOMP0,2==>18MIL
HCOMP1,3==>5MIL

0822
Modify

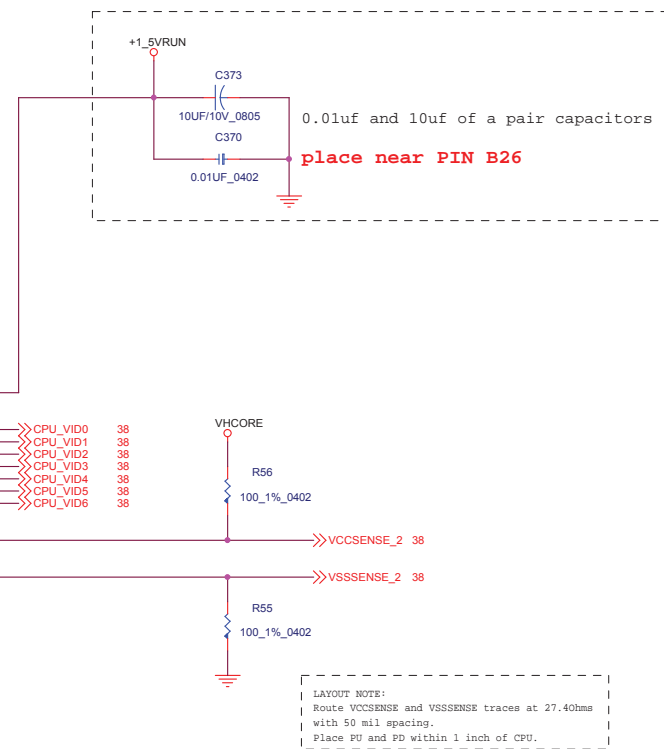
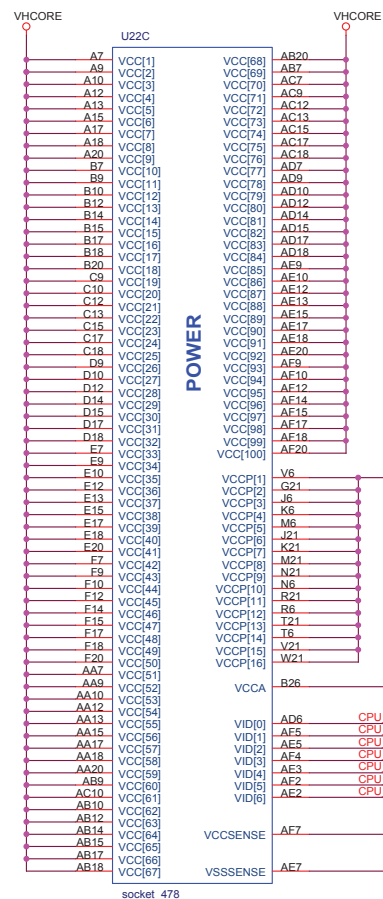
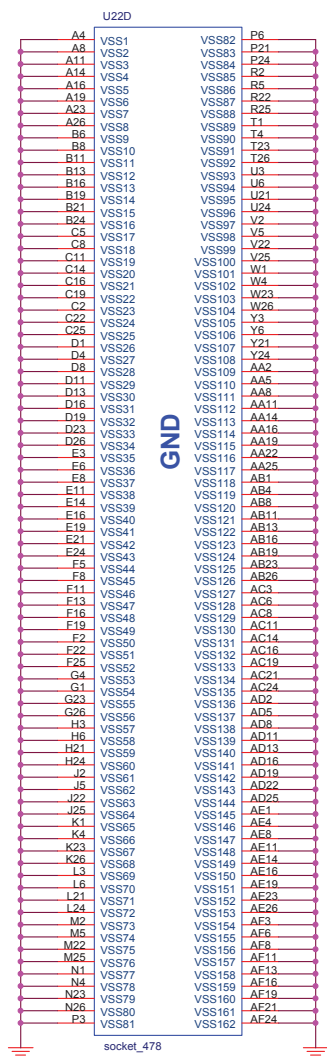


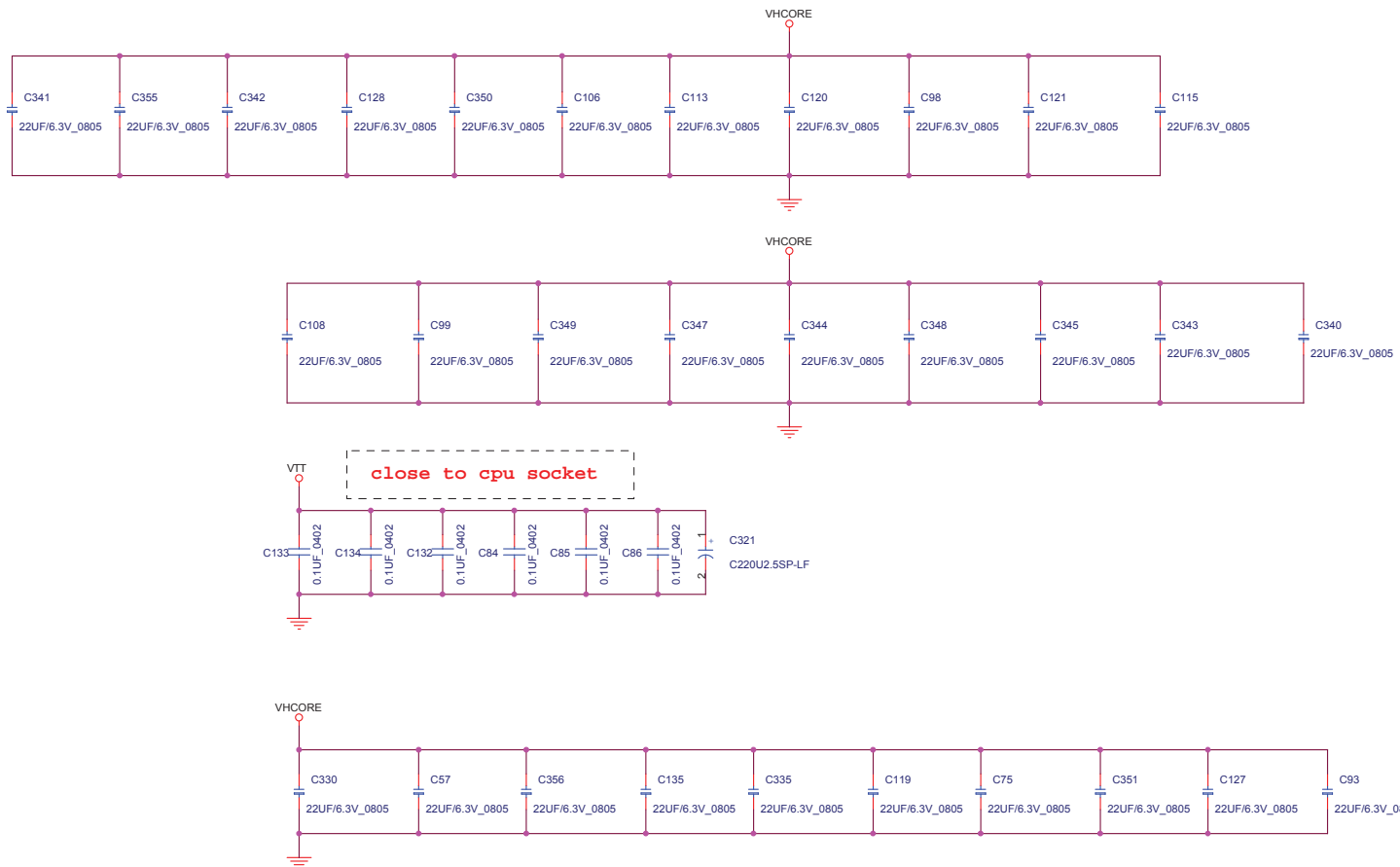
0822
Modify

close thermal
sensor

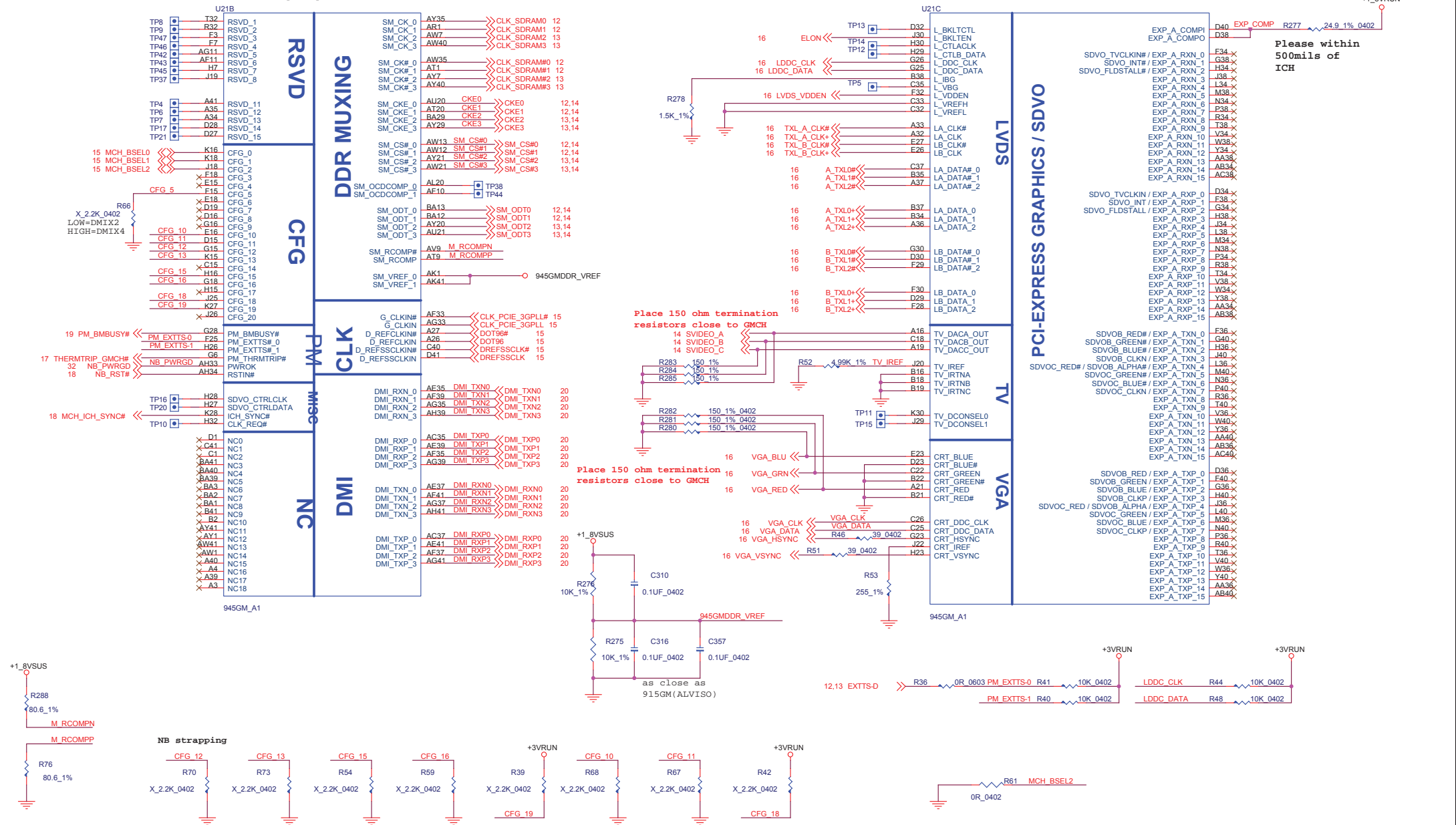


BSEL[2]	BSEL[1]	BSEL[0]	BCLK
L	L	L	RESERVED
L	L	H	133MHZ
L	H	L	RESERVED
L	H	H	166MHZ

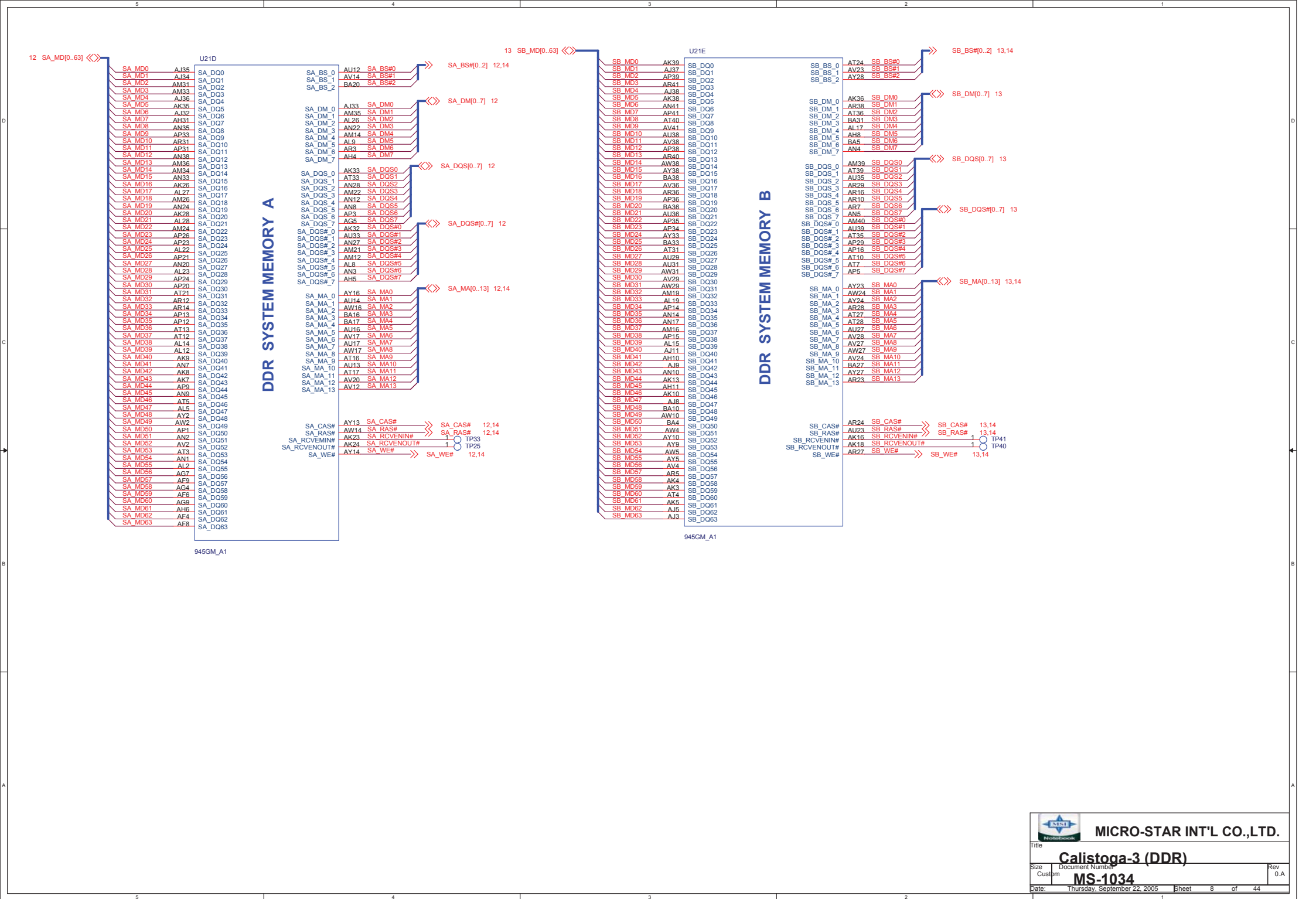




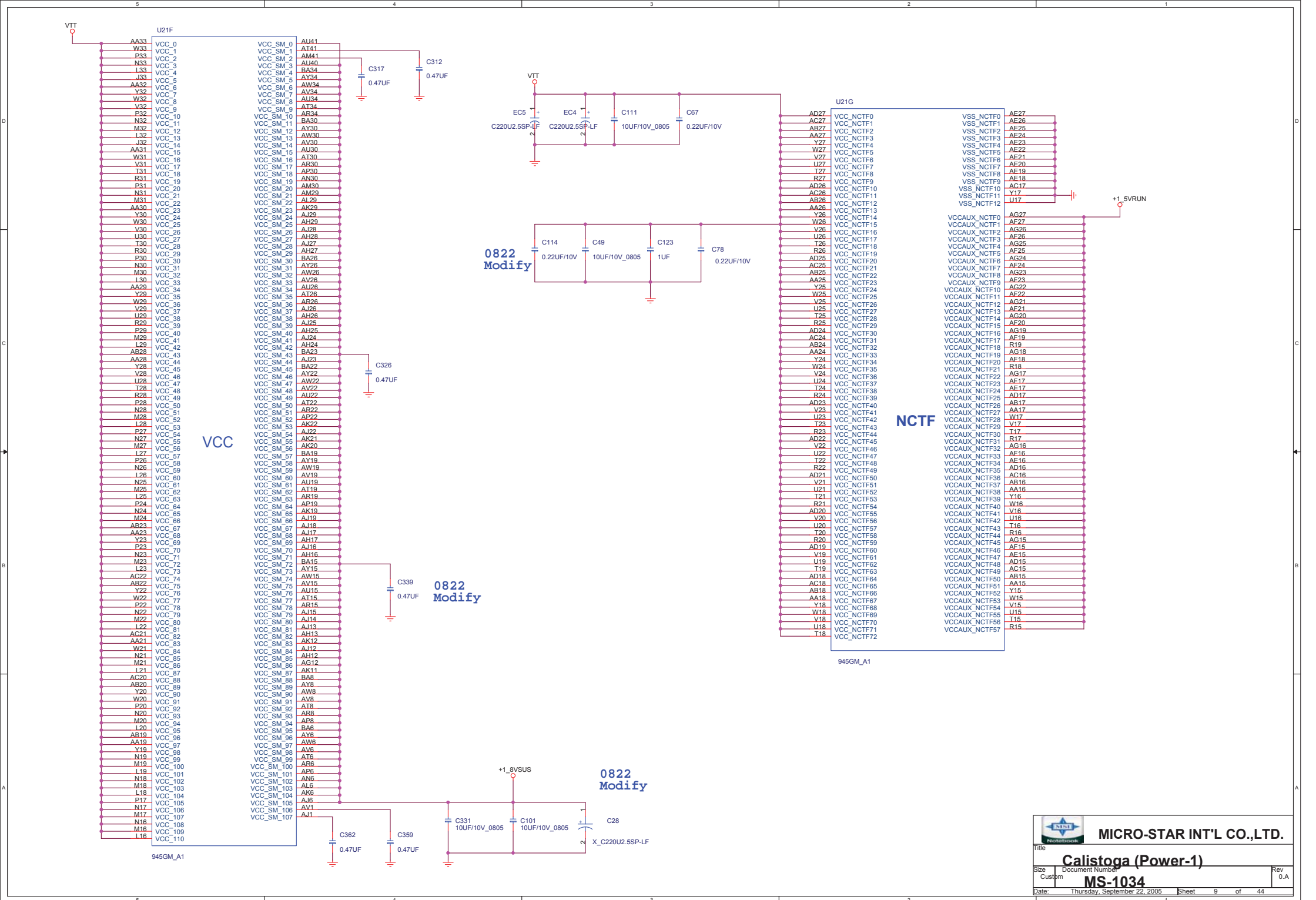
CFG[3:17] Internal Pull up
CFG[18:19] Internal Pull down

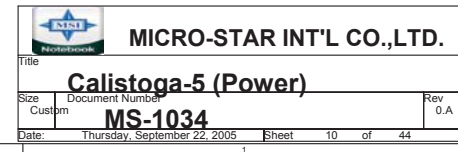


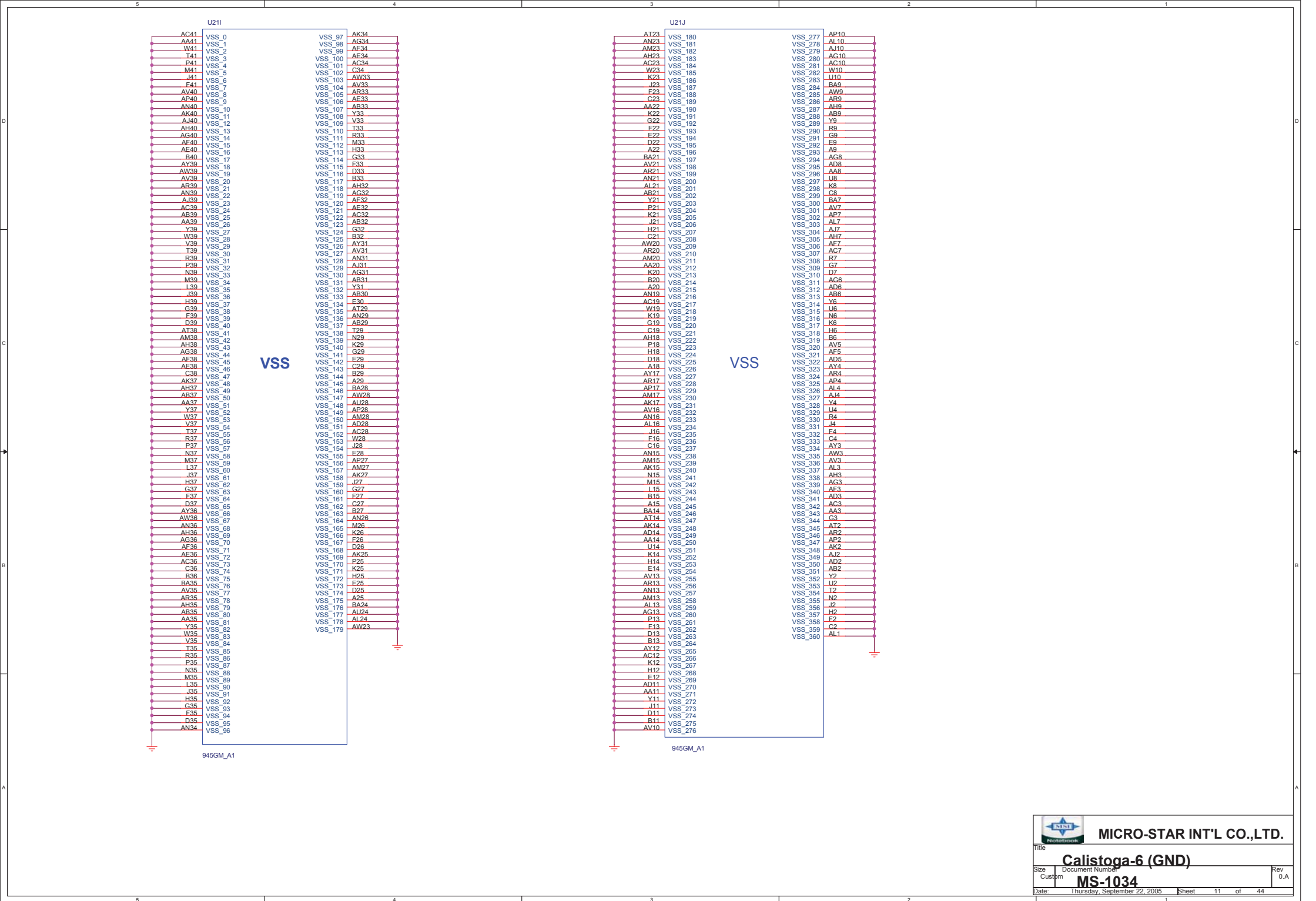
CFG2~0	CFG4~3	CFG5	CFG6	CFG7	CFG8,10,11 14,15,17	CFG9	CFG16	CFG18	CFG19
001=FSB533 011=FSB667	RES	0=DMI x 2 1=DMI x 4 (default)	0=Moby Dick 1=Calistoga	0=Res 1=Mobile CPU	RES	0=reverse 1=normal PCI-E Graphic lane	0=disable 1=enable FSB dynamic ODT	0=1.05V 1=1.5V (default)	0=normal 1=reverse DMI lane reverse
	IPU	IPU	IPU	IPU	IPU	IPU	IPU	IPD	IPD



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SA MD0	5	DO0	A0	102	SA MA0
SA MD1	7	DO1	A1	101	SA MA1
SA MD2	17	DO2	A2	100	SA MA2
SA MD3	19	DO3	A4	99	SA MA3
SA MD4	4	DO4	A5	98	SA MA4
SA MD5	6	DO5	A6	97	SA MA5
SA MD6	14	DO6	A7	94	SA MA6
SA MD7	16	DO7	A8	92	SA MA7
SA MD8	23	DO8	A9	93	SA MA8
SA MD9	25	DO9	A10/AP	91	SA MA9
SA MD10	35	DO10	A11	105	SA MA10
SA MD11	37	DO11	A12	90	SA MA11
SA MD12	20	DO12	A13	89	SA MA12
SA MD13	22	DO13	A14	116	SA MA13
SA MD14	36	DO14	A15	86	X
SA MD15	38	DO15	A16_BA2	84	X
SA MD16	43	DO16		85	SA BS#2
SA MD17	45	DO17			
SA MD18	55	DO18	BA0	107	SA BS#0
SA MD19	57	DO19	BA1	106	SA BS#1
SA MD20	44	DO20	S0#	110	SM CS#0
SA MD21	46	DO21	S1#	115	SM CS#1
SA MD22	56	DO22	CK0	30	CLK SDRAM0
SA MD23	58	DO23	CK0#	32	CLK SDRAM#0
SA MD24	61	DO24	CK1	164	CLK SDRAM1
SA MD25	63	DO25	CK1#	166	CLK SDRAM#1
SA MD26	73	DO26	CKE0	79	CKE0
SA MD27	75	DO27	CKE1	80	CKE1
SA MD28	62	DO28	CAS#	113	SA CAS#
SA MD29	64	DO29	RAS#	108	SA RAS#
SA MD30	74	DO30	WE#	109	SA WE#
SA MD31	76	DO31	SA0	198	SA SA0
SA MD32	123	DO32	SA1	200	SA SA1
SA MD33	125	DO33	SCL	197	RUN_SMBCLK
SA MD34	135	DO34	SDA	195	RUN_SMBDATA
SA MD35	137	DO35			
SA MD36	124	DO36	ODT0	114	SM ODT0
SA MD37	126	DO37	ODT1	119	SM ODT1
SA MD38	134	DO38			
SA MD39	136	DO39	DM0	10	SA DM0
SA MD40	141	DO40	DM1	26	SA DM1
SA MD41	143	DO41	DM2	52	SA DM2
SA MD42	151	DO42	DM3	67	SA DM3
SA MD43	153	DO43	DM4	130	SA DM4
SA MD44	140	DO44	DM5	147	SA DM5
SA MD45	142	DO45	DM6	170	SA DM6
SA MD46	152	DO46	DM7	185	SA DM7
SA MD47	154	DO47			
SA MD48	157	DO48	DQS0	13	SA DQS0
SA MD49	159	DO49	DQS1	31	SA DQS1
SA MD50	173	DO50	DQS2	51	SA DQS2
SA MD51	175	DO51	DQS3	70	SA DQS3
SA MD52	158	DO52	DQS4	131	SA DQS4
SA MD53	160	DO53	DQS5	148	SA DQS5
SA MD54	174	DO54	DQS6	169	SA DQS6
SA MD55	176	DO55	DQS7	188	SA DQS7
SA MD56	179	DO56	DQS#0	11	SA DQS#0
SA MD57	181	DO57	DQS#1	29	SA DQS#1
SA MD58	189	DO58	DQS#2	49	SA DQS#2
SA MD59	191	DO59	DQS#3	68	SA DQS#3
SA MD60	180	DO60	DQS#4	129	SA DQS#4
SA MD61	182	DO61	DQS#5	146	SA DQS#5
SA MD62	192	DO62	DQS#6	167	SA DQS#6
SA MD63	194	DO63	DQS#7	186	SA DQS#7

CN6A

DDR2_SODIMM_STD_H=5.2mm

SA MD[0..63] <<> SA_MD[0..63] 8
 SA DM[0..7] <<> SA_DM[0..7] 8
 SA DQS[0..7] <<> SA_DQS[0..7] 8
 SA DQS#0..7 <<> SA_DQS#[0..7] 8
 SA MA[0..13] <<> SA_MA[0..13] 8,14
 SA BS#0..21 <<> SA_BS#[0..21] 8,14

0822
Modify

+3VVRUN

C145

2.2UF/6.3V

C143

0.1UF_0402

7,13

EXTTS-D <<>

SMDDDR_VREF

C21

2.2UF/6.3V

C19

0.1UF_0402



+1_8VSUS

CN6B

VDD1

VDD2

VDD3

VDD4

VDD5

VDD6

VDD7

VDD8

VDD9

VDD10

VDD11

VDD12

VDDSPD

VSS16

VSS17

VSS18

VSS19

VSS20

VSS21

VSS22

VSS23

VSS24

VSS25

VSS26

VSS27

VSS28

VSS29

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VSS210

VSS211

VSS212

VSS213

VSS214

VSS215

VSS216

VSS217

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VSS223

VSS224

VSS225

VSS226

VSS227

VSS228

V

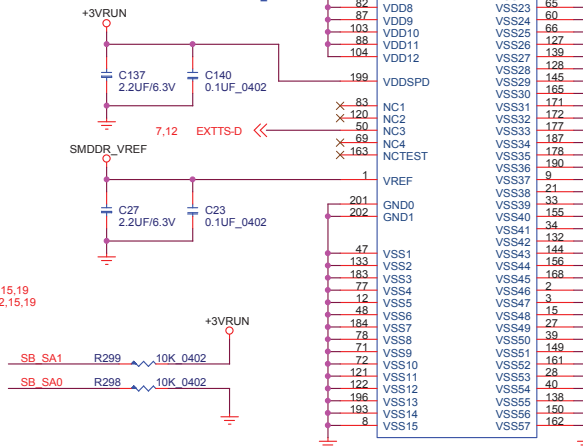
need update
footprint

SB MD0	5	DO0	A0	102	SB MA0
SB MD1	7	DO1	A1	101	SB MA1
SB MD2	17	DO2	A2	100	SB MA2
SB MD3	19	DO3	A3	99	SB MA3
SB MD4	4	DO4	A4	98	SB MA4
SB MD5	6	DO5	A5	97	SB MA5
SB MD6	14	DO6	A6	94	SB MA6
SB MD7	16	DO7	A7	92	SB MA7
SB MD8	23	DO8	A8	93	SB MA8
SB MD9	25	DO9	A9	91	SB MA9
SB MD10	35	DO10	A10/AP	105	SB MA10
SB MD11	37	DO11	A11	89	SB MA11
SB MD12	20	DO12	A12	89	SB MA12
SB MD13	22	DO13	A13	116	SB MA13
SB MD14	36	DO14	A14	86	X
SB MD15	38	DO15	A15	84	X
SB MD16	43	DO16	A16_BA2	85	SB BS#2
SB MD17	45	DO17			
SB MD18	55	DO18	BA0	107	SB BS#0
SB MD19	57	DO19	BA1	106	SB BS#1
SB MD20	44	DO20	SO#	110	SM CS#2
SB MD21	46	DO21	CK0	115	SM CS#3
SB MD22	56	DO22	CK1	30	CLK SDRAM3
SB MD23	58	DO23	CK2	32	CLK SDRAM#3
SB MD24	61	DO24	CK3	154	CLK SDRAM2
SB MD25	63	DO25	CK4	156	CLK SDRAM#2
SB MD26	73	DO26	CK5	79	CKE2
SB MD27	75	DO27	CK6	80	CKE3
SB MD28	62	DO28	CAS#	113	SB CAS#
SB MD29	64	DO29	RAS#	108	SB RAS#
SB MD30	74	DO30	WE#	109	SB WE#
SB MD31	76	DO31	SA0	198	SB SA0
SB MD32	123	DO32	SA1	200	SB SA1
SB MD33	125	DO33	SCL	197	RUN_SMBCLK
SB MD34	135	DO34	SDA	195	RUN_SMBDATA
SB MD35	137	DO35			
SB MD36	124	DO36	ODT0	114	SM ODT2
SB MD37	126	DO37	ODT1	119	SM ODT3
SB MD38	134	DO38			
SB MD39	136	DO39	DM0	10	SB DM0
SB MD40	141	DO40	DM1	26	SB DM1
SB MD41	143	DO41	DM2	52	SB DM2
SB MD42	151	DO42	DM3	67	SB DM3
SB MD43	153	DO43	DM4	130	SB DM4
SB MD44	140	DO44	DM5	147	SB DM5
SB MD45	142	DO45	DM6	170	SB DM6
SB MD46	152	DO46	DM7	185	SB DM7
SB MD47	154	DO47			
SB MD48	157	DO48	DQS0	13	SB DQS0
SB MD49	159	DO49	DQS1	31	SB DQS1
SB MD50	173	DO50	DQS2	51	SB DQS2
SB MD51	175	DO51	DQS3	70	SB DQS3
SB MD52	158	DO52	DQS4	131	SB DQS4
SB MD53	160	DO53	DQS5	148	SB DQS5
SB MD54	174	DO54	DQS6	169	SB DQS6
SB MD55	176	DO55	DQS7	188	SB DQS7
SB MD56	179	DO56	DQS#0	11	SB DQS#0
SB MD57	181	DO57	DQS#1	29	SB DQS#1
SB MD58	189	DO58	DQS#2	49	SB DQS#2
SB MD59	191	DO59	DQS#3	68	SB DQS#3
SB MD60	180	DO60	DQS#4	129	SB DQS#4
SB MD61	182	DO61	DQS#5	146	SB DQS#5
SB MD62	192	DO62	DQS#6	167	SB DQS#6
SB MD63	194	DO63	DQS#7	186	SB DQS#7

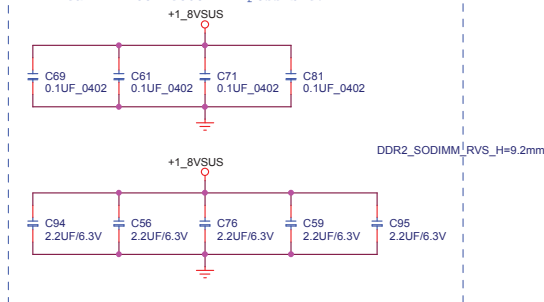
DDR2_SODIMM_RVS_H=9.2mm

SB MD[0..63] <<> SB_MD[0..63] 8
SB DM[0..7] <<> SB_DM[0..7] 8
SB DQS[0..7] <<> SB_DQS[0..7] 8
SB DQS#0..7 <<> SB_DQS#[0..7] 8
SB MA[0..13] <<> SB_MA[0..13] 8,14
SB BS#0..21 <<> SB_BS#[0..21] 8,14

0822
Modify



Layout note: Place capacitors between and
near DDR connector if possible.

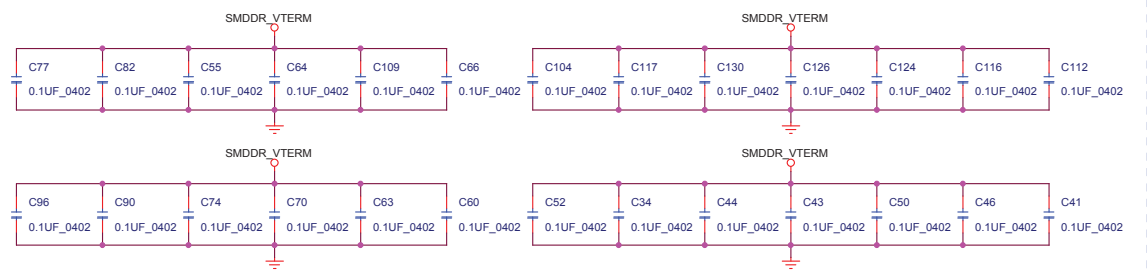
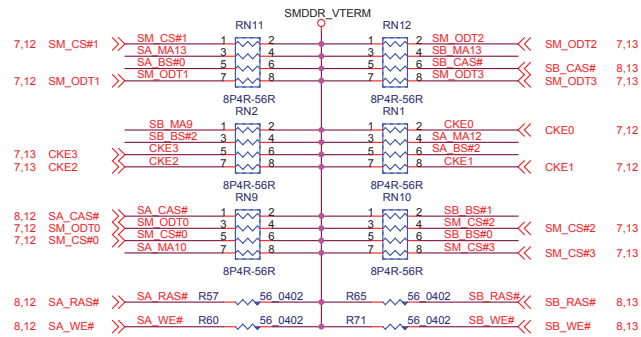
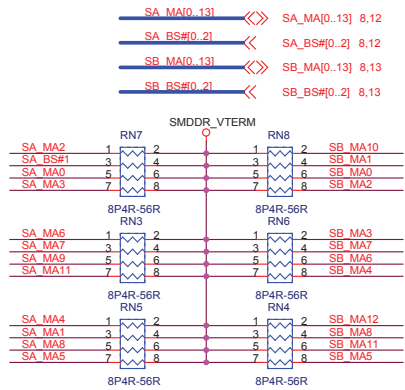


DDR2_SODIMM_RVS_H=9.2mm

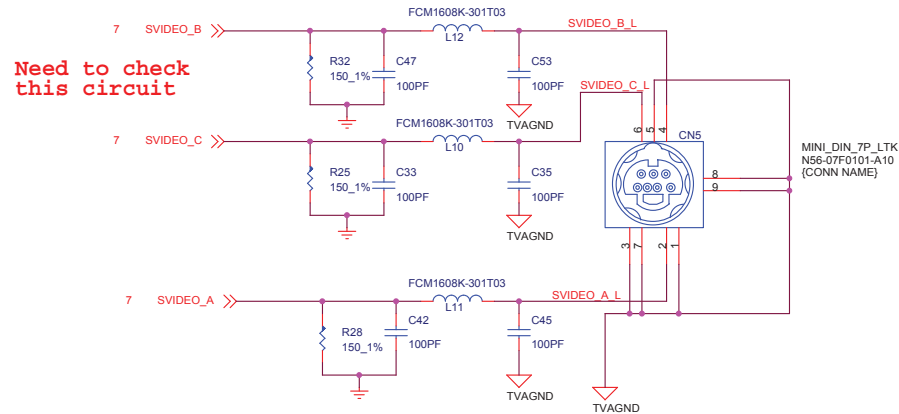
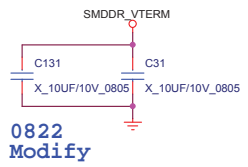


MICRO-STAR INT'L CO.,LTD.

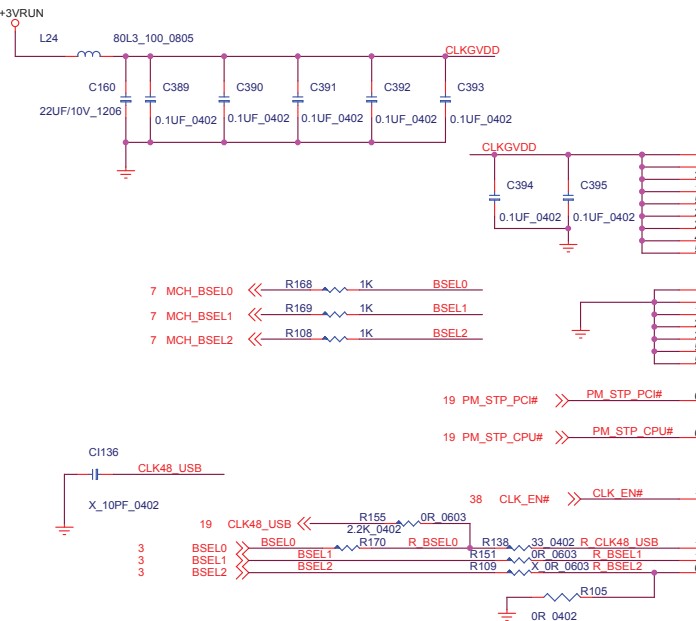
Title	Document Number	Rev
DDR2-SODIMM-1 (Channel B)	MS-1034	0.A
Size	Custom	
Date:	Thursday, September 22, 2005	Sheet 13 of 44



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V.



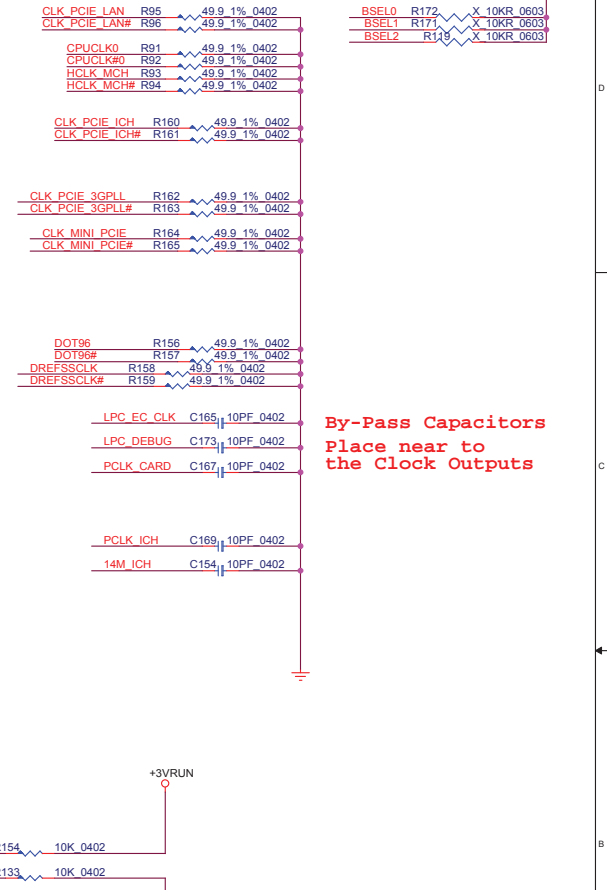
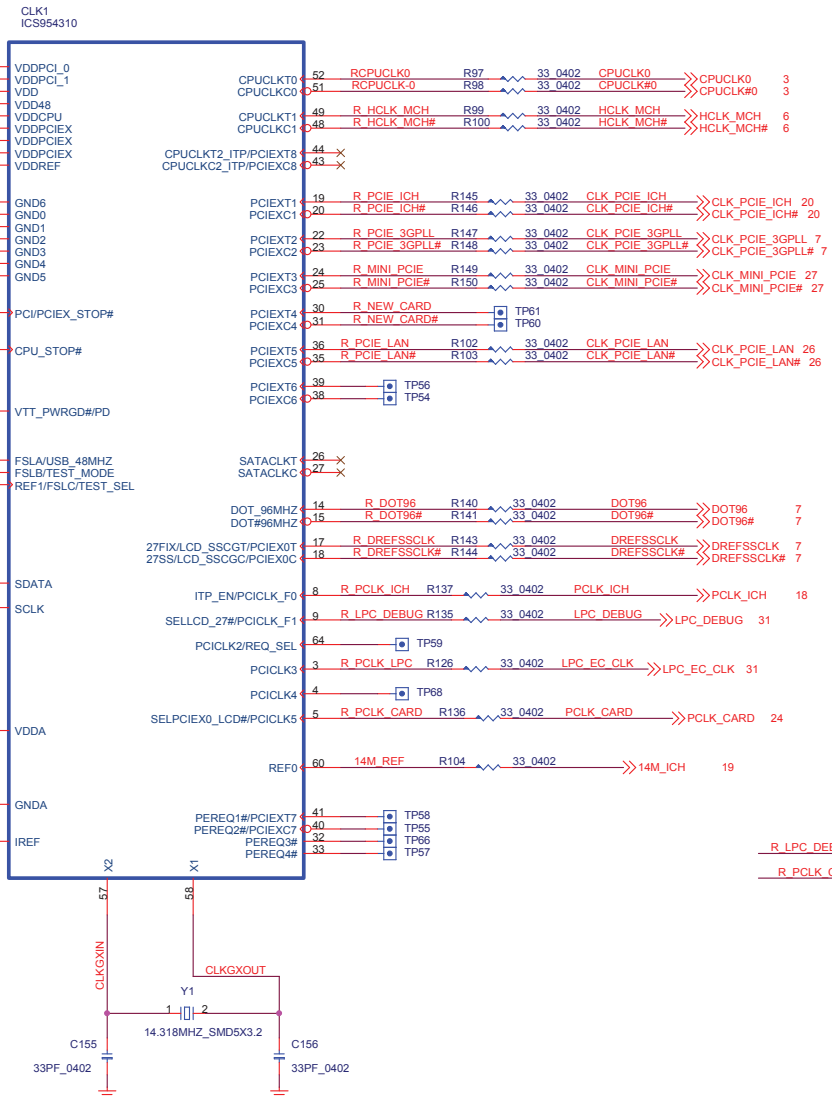
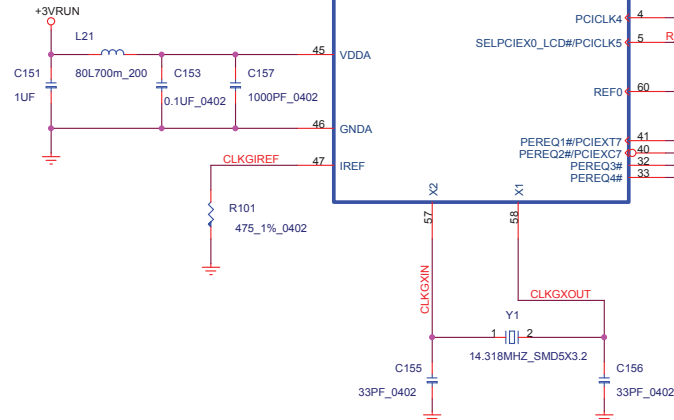
Need to check this circuit



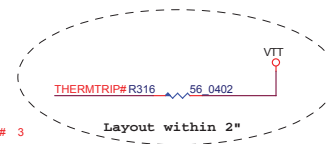
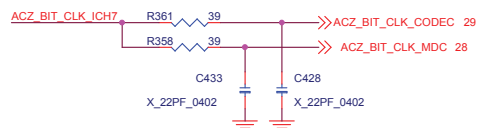
CPU Table			
BSEL[2]	BSEL[1]	BSEL[0]	BCLK
L	L	L	RESERVED
L	L	H	133MHZ
L	H	L	RESERVED
L	H	H	166MHZ

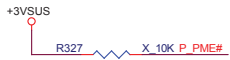
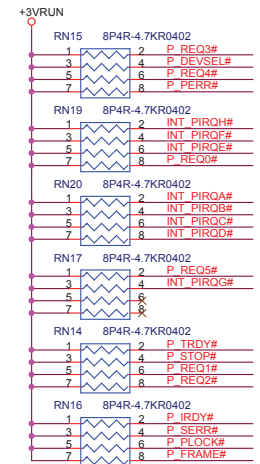
CLOCK GEN Table			
FSLC (BSEL2)	FSLB (BSEL1)	FSLA (BSEL0)	CPU Mhz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	200.00

12,13,19 RUN_SMBDATA <<> RUN_SMBDATA 55
12,13,19 RUN_SMBCLK <<> RUN_SMBCLK 54



By-Pass Capacitors
Place near to
the Clock Outputs





0822
Modify

24 P_AD[0..31]

U24B

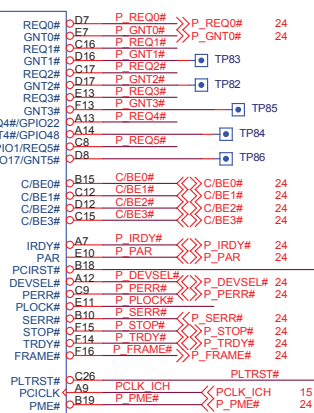
PCI

ICH7-M
PARTB

Interrupt I/F

MISC

ICH7-M_A1



0822
Modify

PCI_RST#

+3VSUS

0822
Modify

+3VSUS

0822
Modify

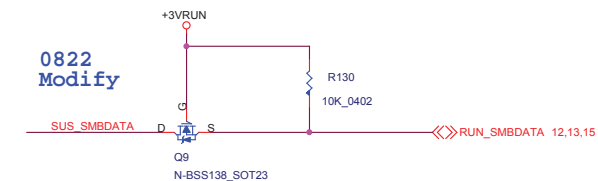
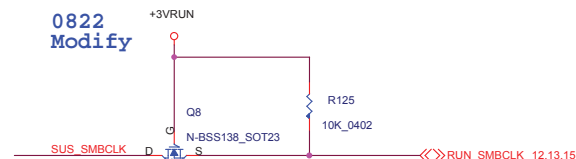
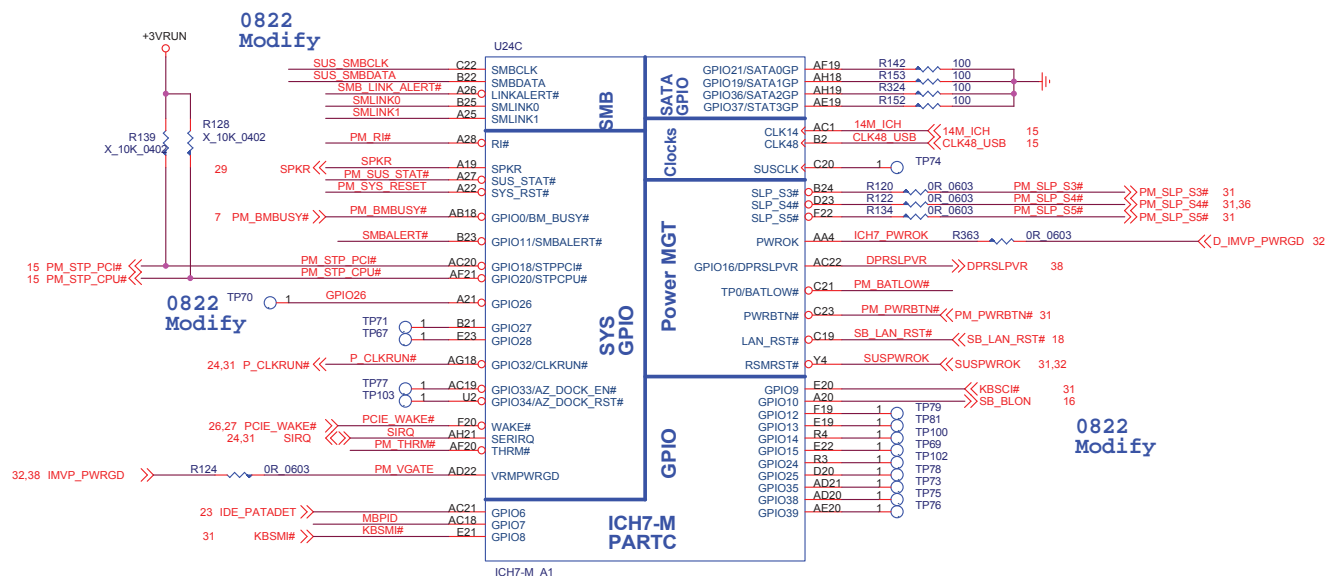
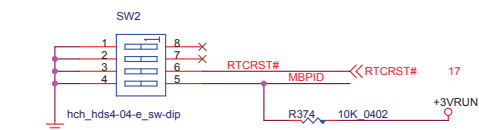
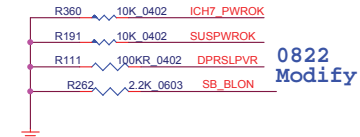
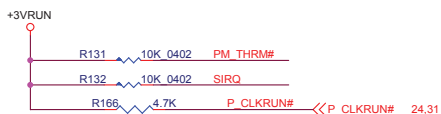
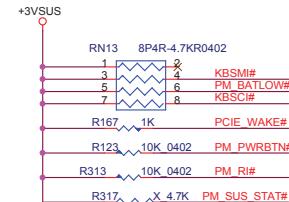
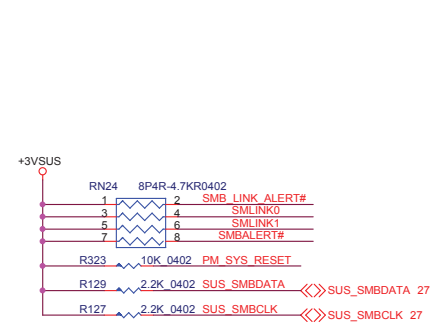
+3VSUS

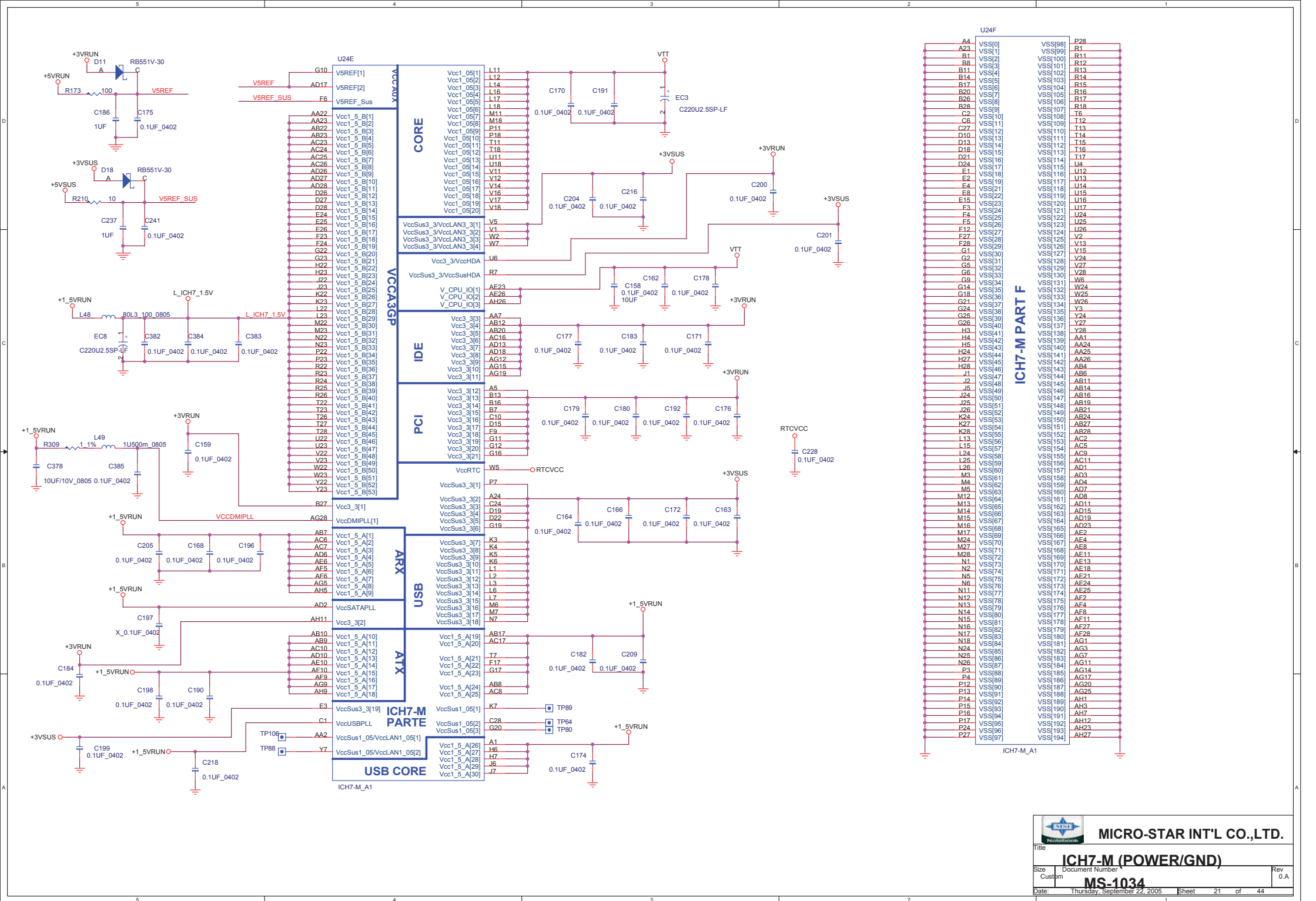
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LPC(D)	H	H
PCI	L	H
SPI	H	L

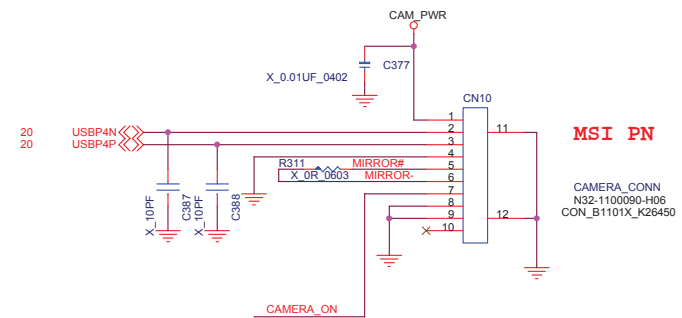
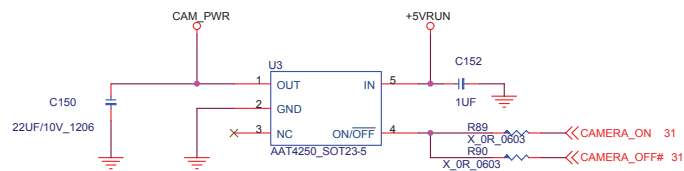
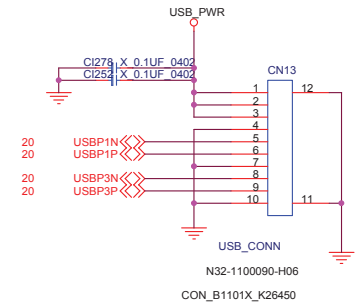
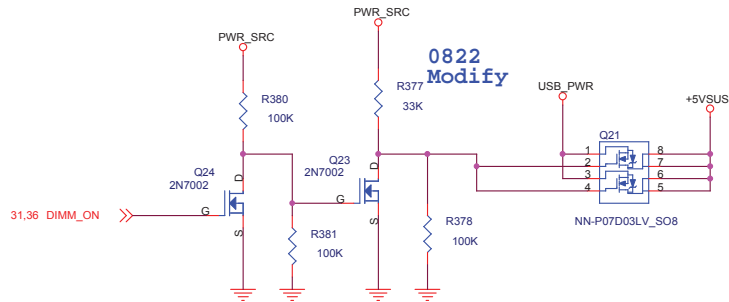
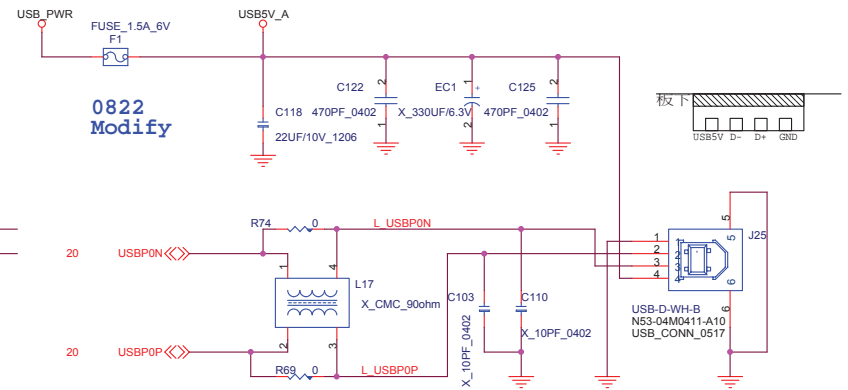
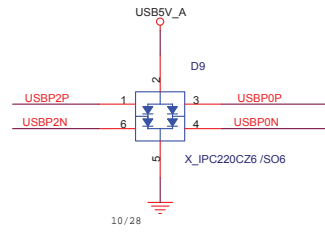
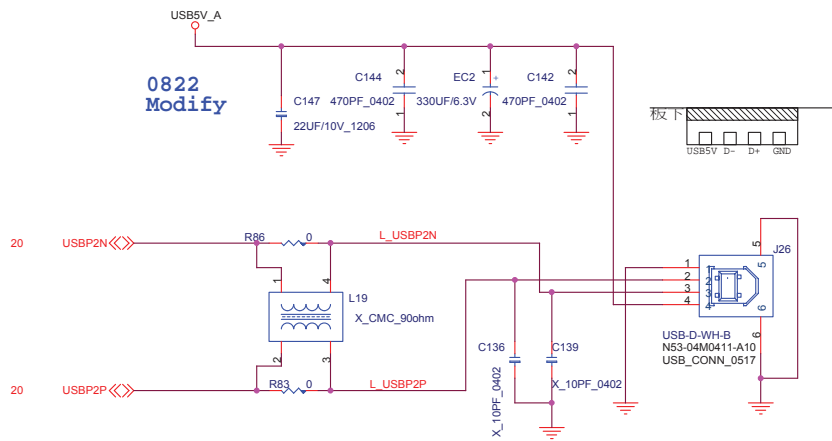


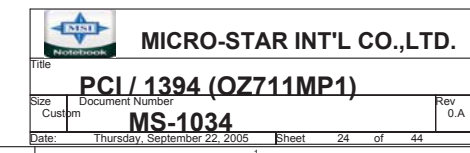
MICRO-STAR INT'L CO.,LTD.

Title		ICH7-M (PCI BUS)		Rev	
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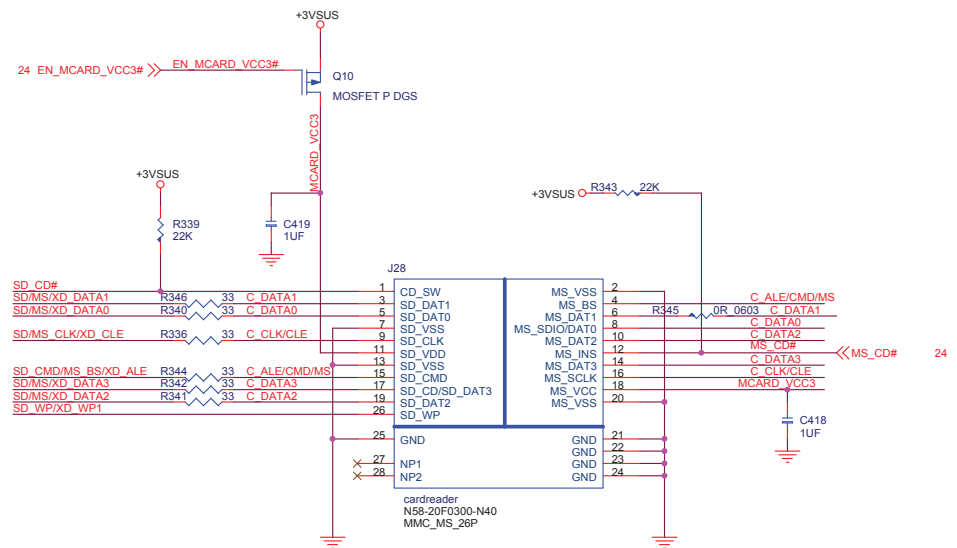
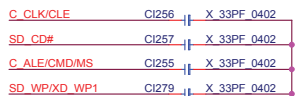
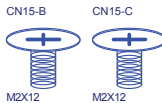
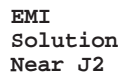
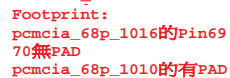




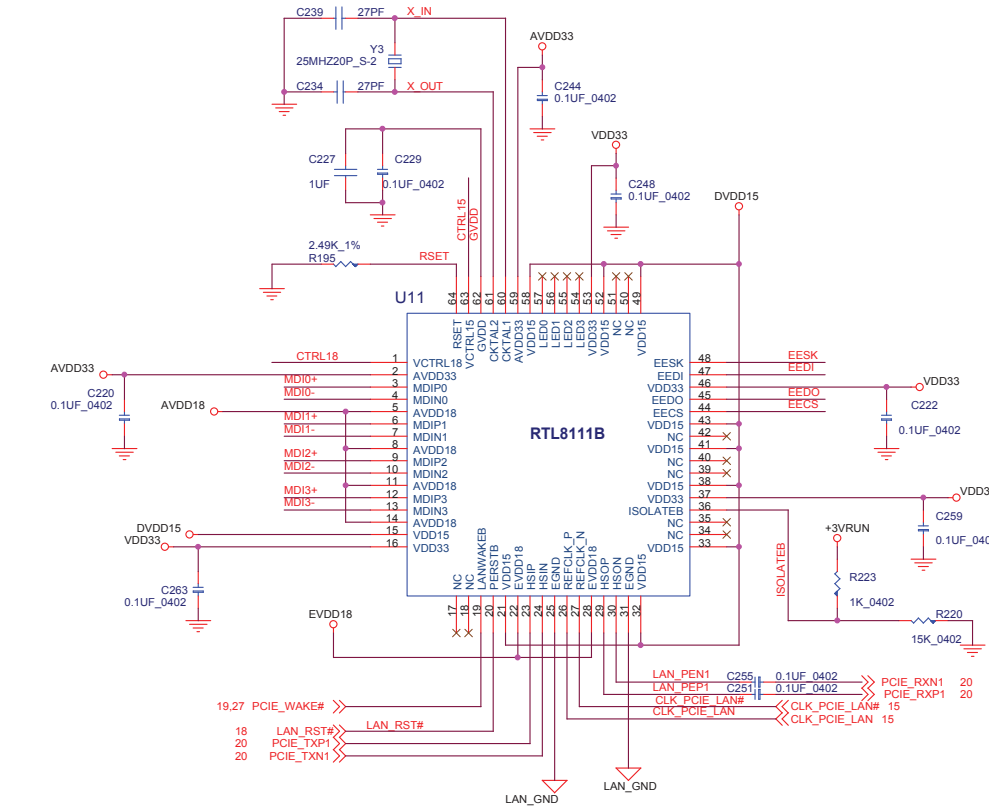
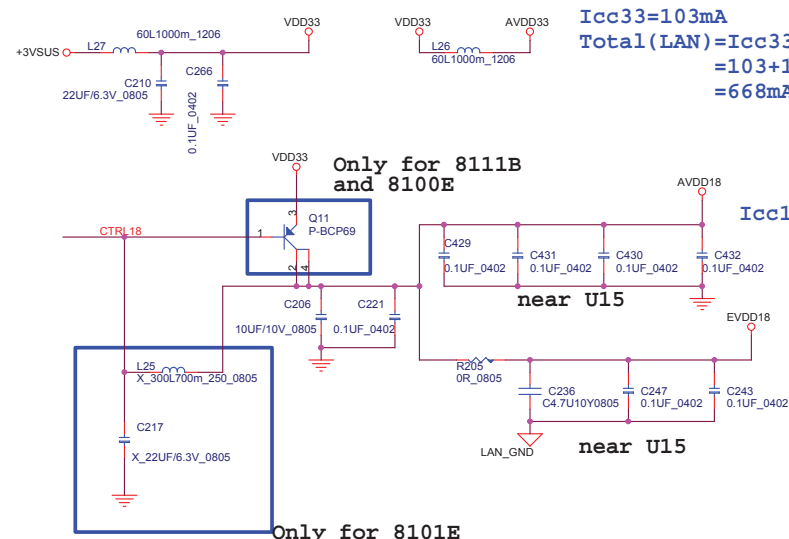
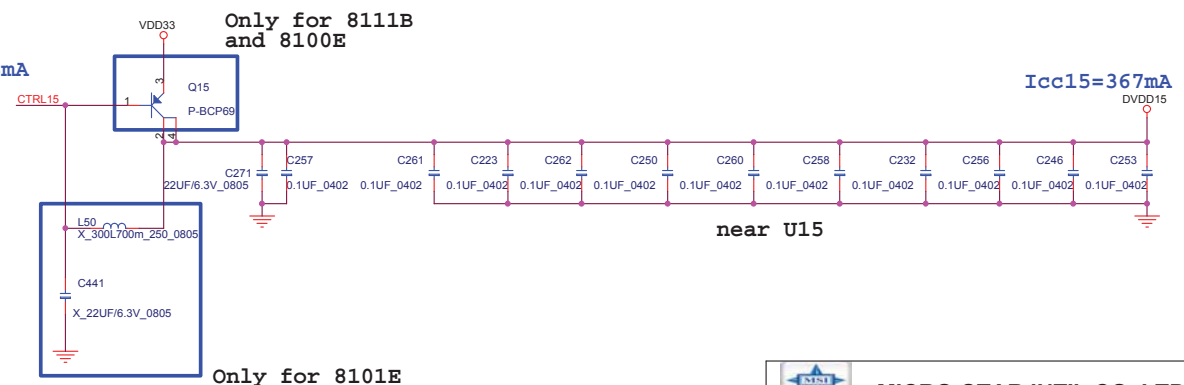




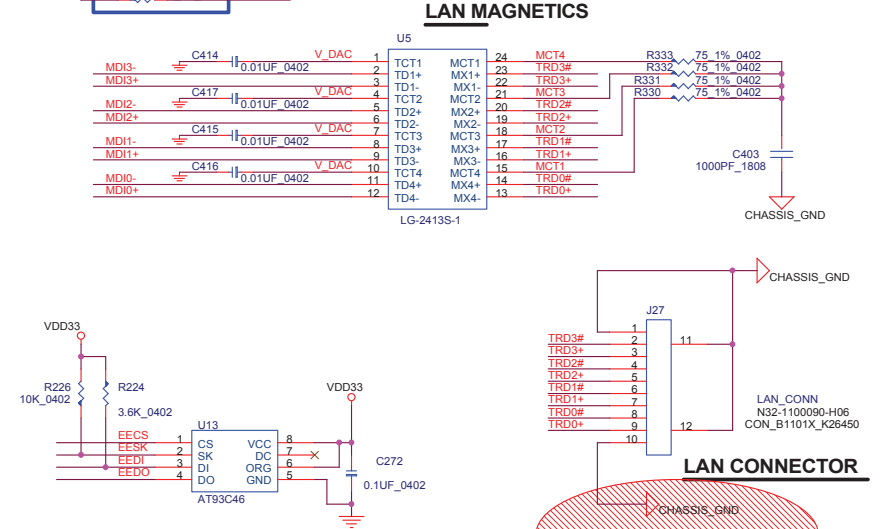
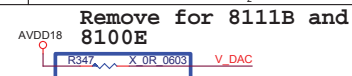
CN15 TAISOL_146-2221210-01_PCMCIA_SMT



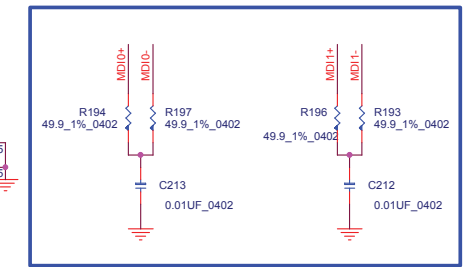
Title			
CARDBUS/FLASH CARD			
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$$\begin{aligned} \text{Icc33} &= 103\text{mA} \\ \text{Total (LAN)} &= \text{Icc33} + \text{Icc18} + \text{Icc15} \\ &= 103 + 198 + 367 \\ &= 668\text{mA} \end{aligned}$$

$$I_{C18} = 198 \text{ mA}$$


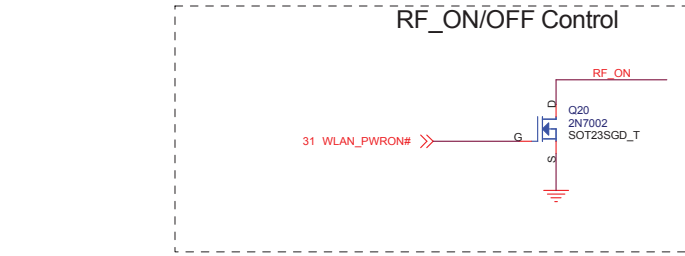
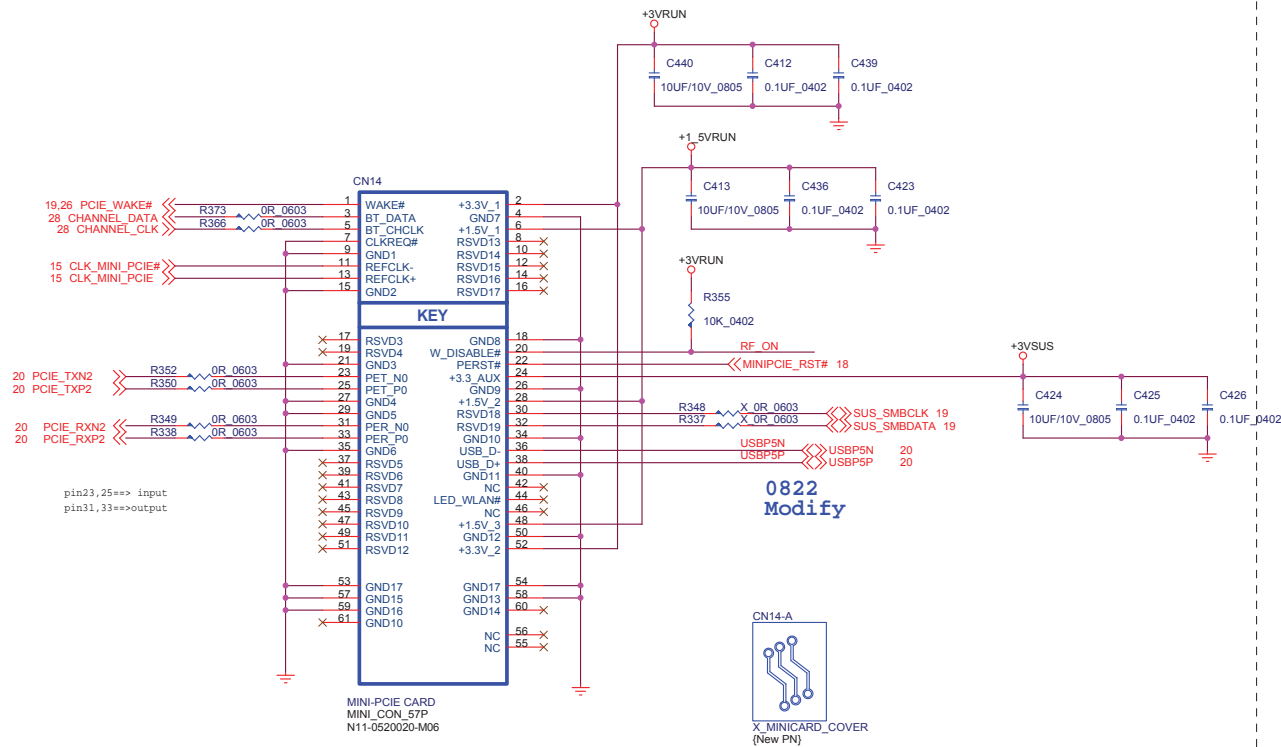
Only for 8101E



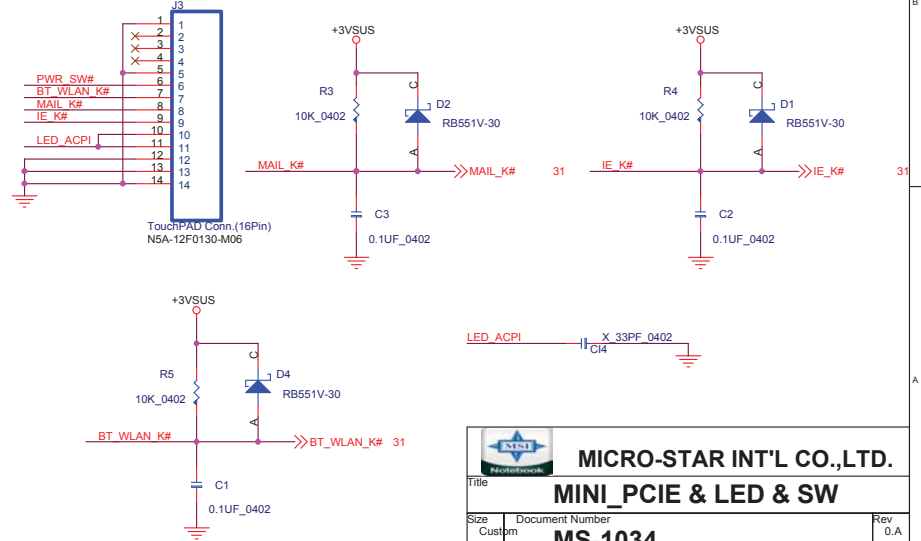
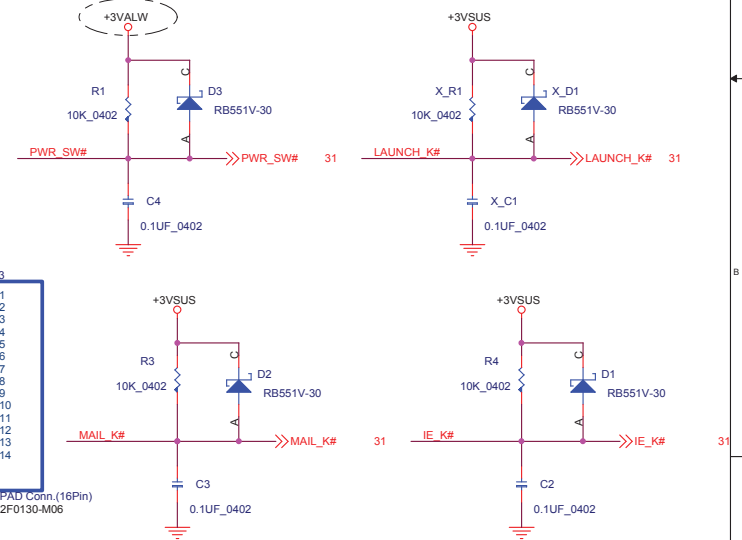
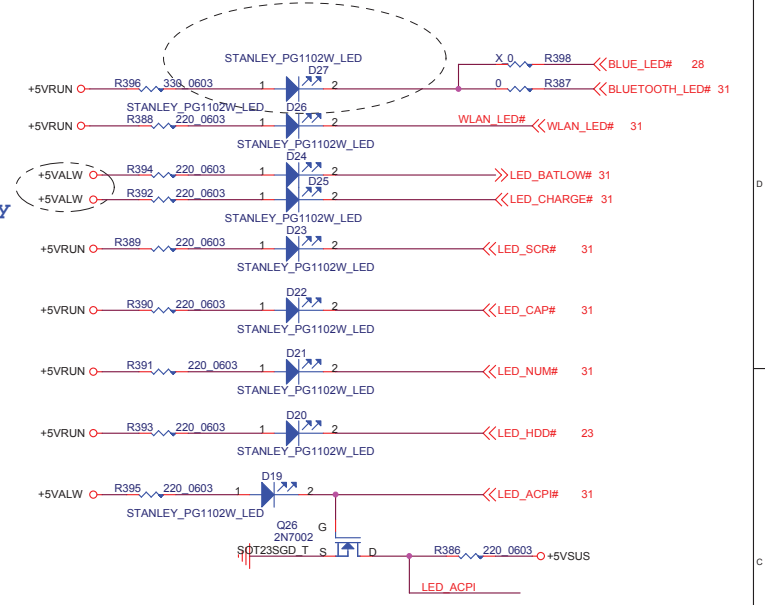
LAN MAGNETICS



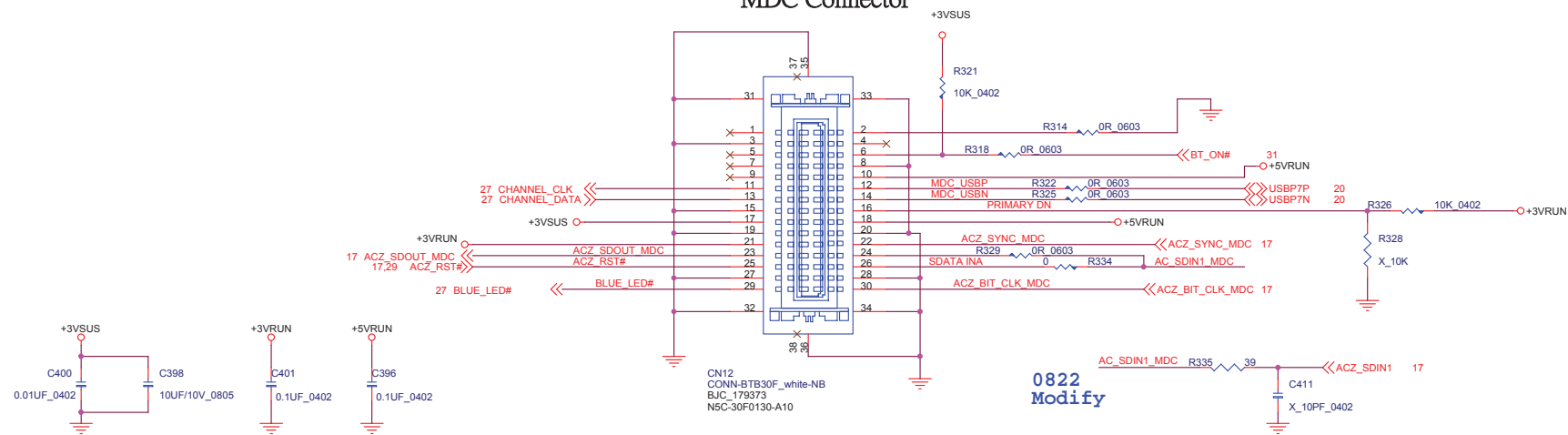
LAN CONNECTOR

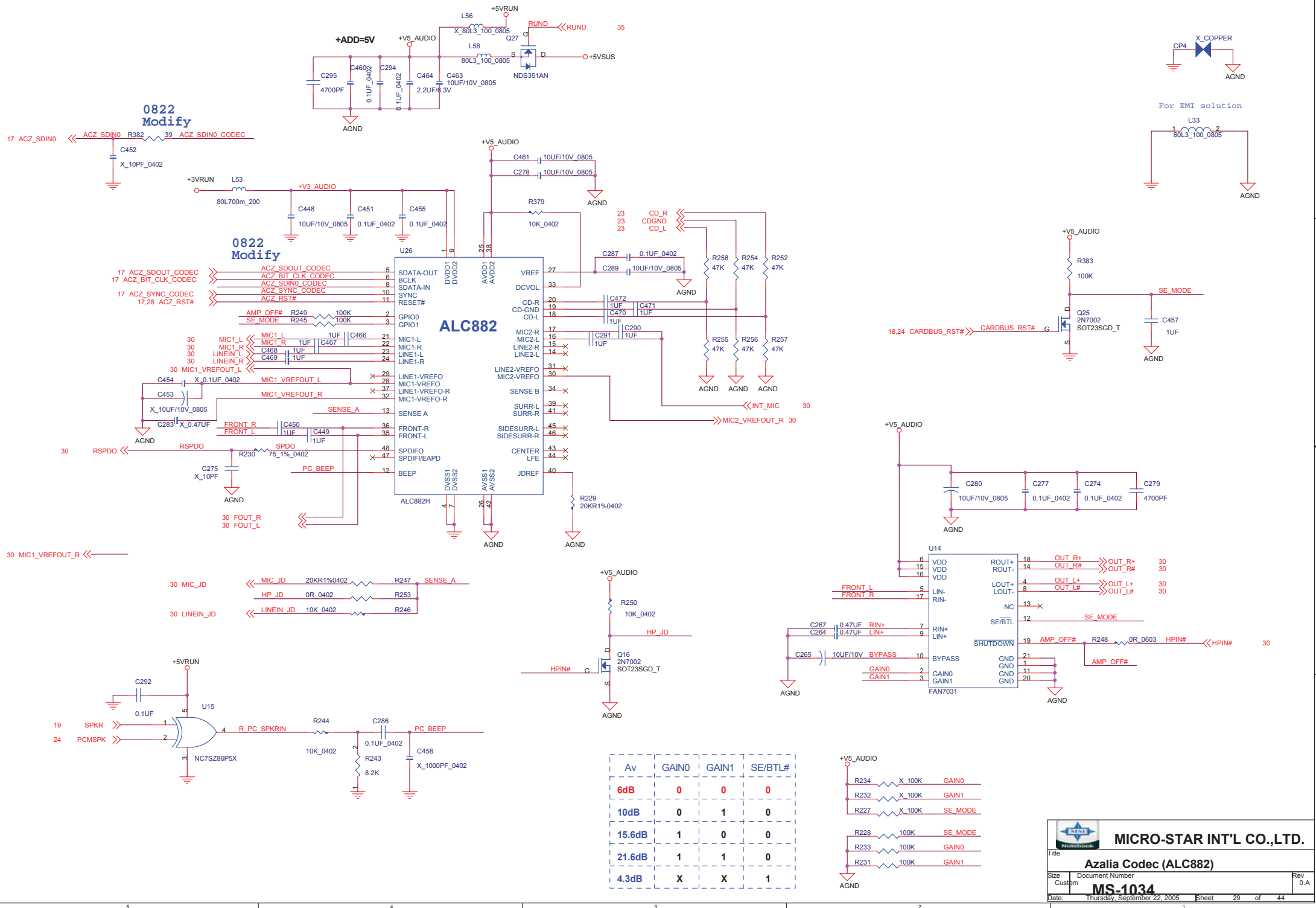


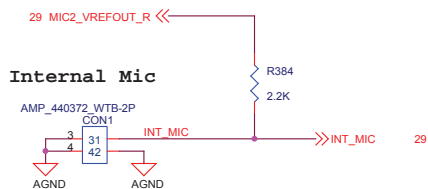
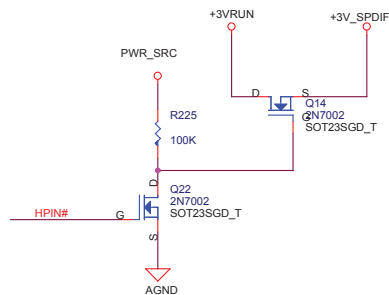
0822
Modify



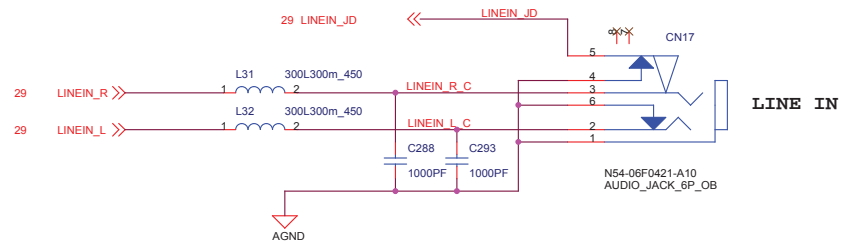
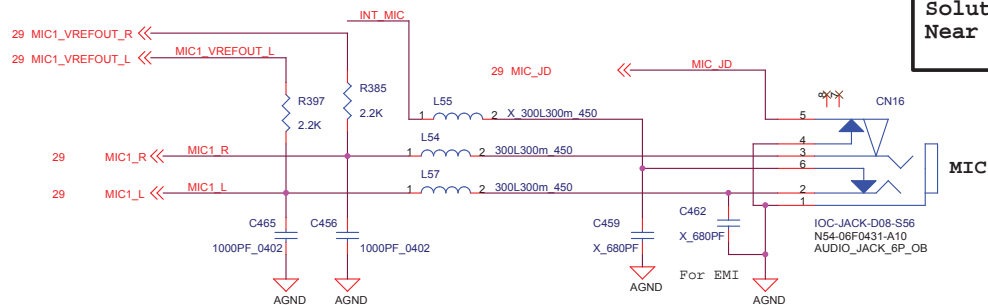
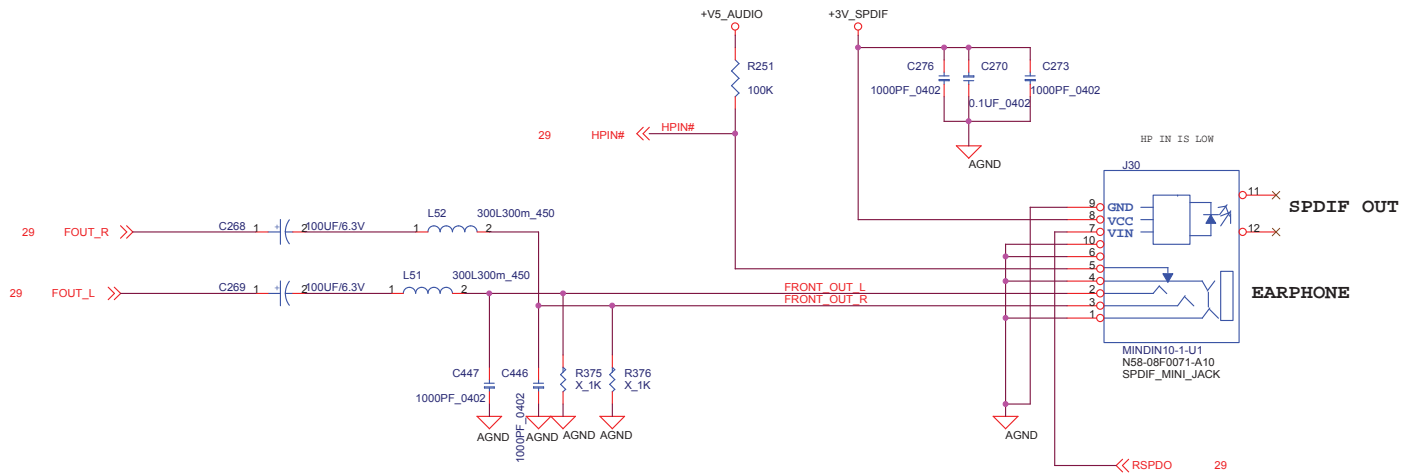
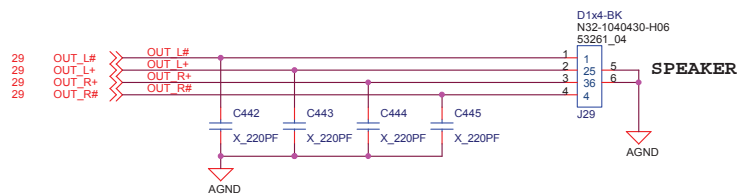
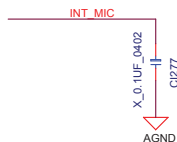
MDC Connector

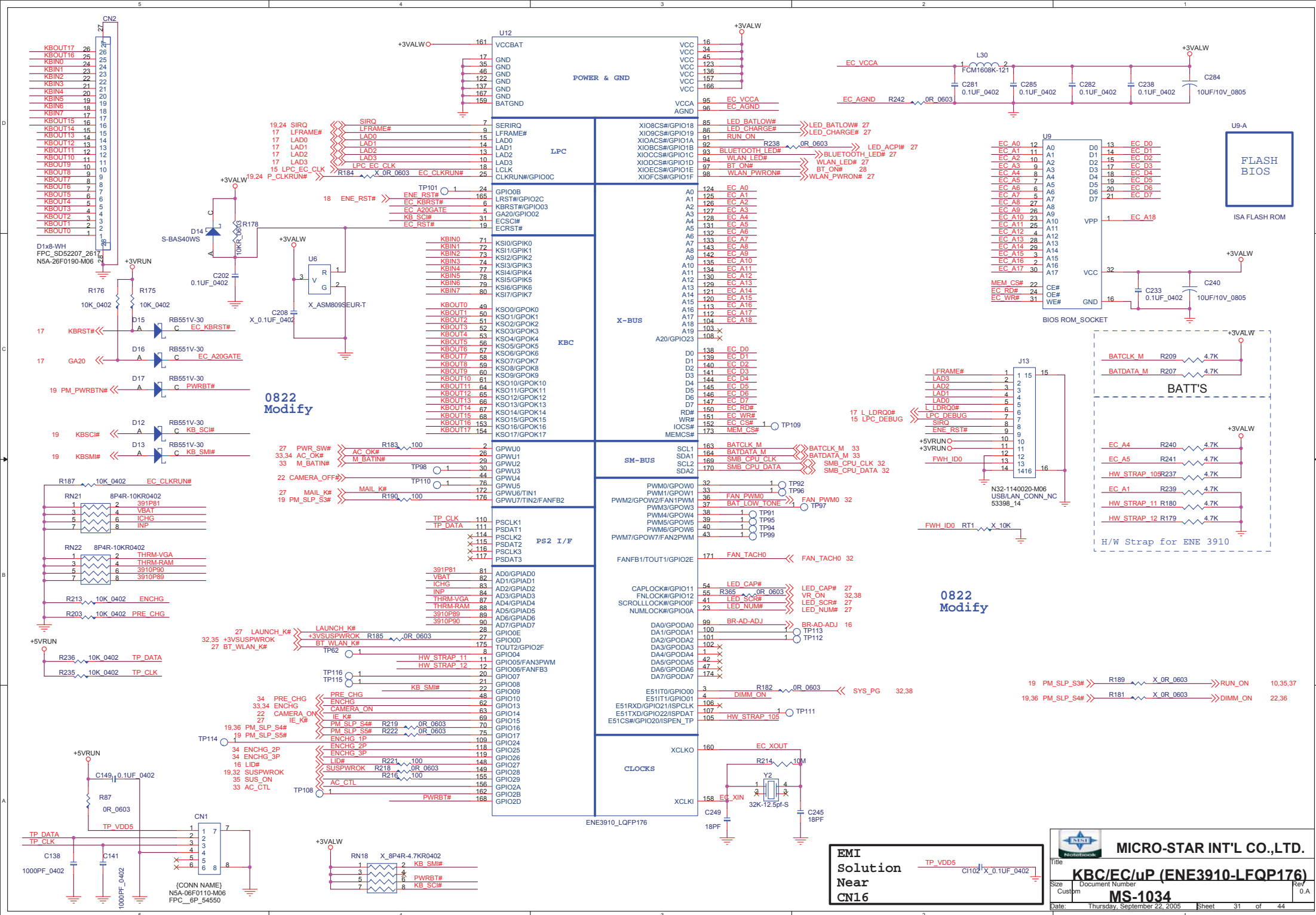


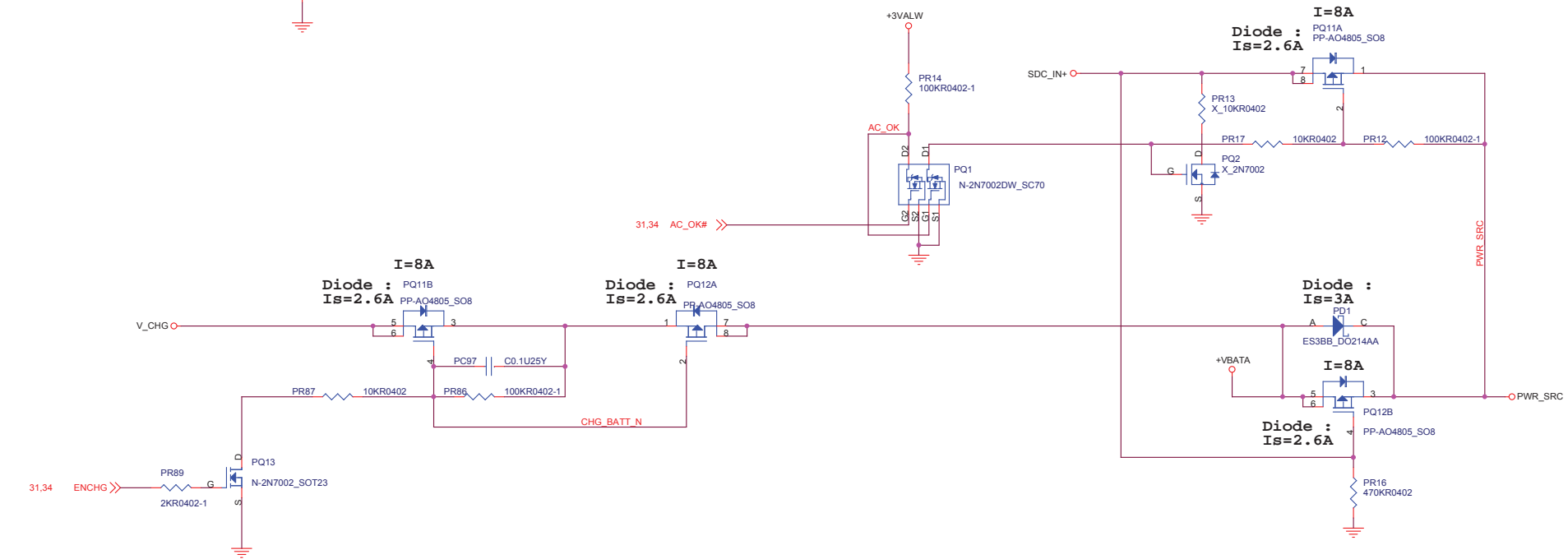
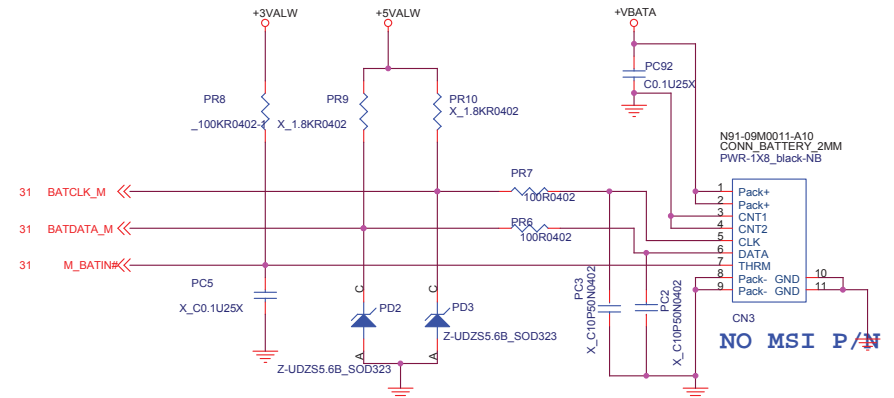
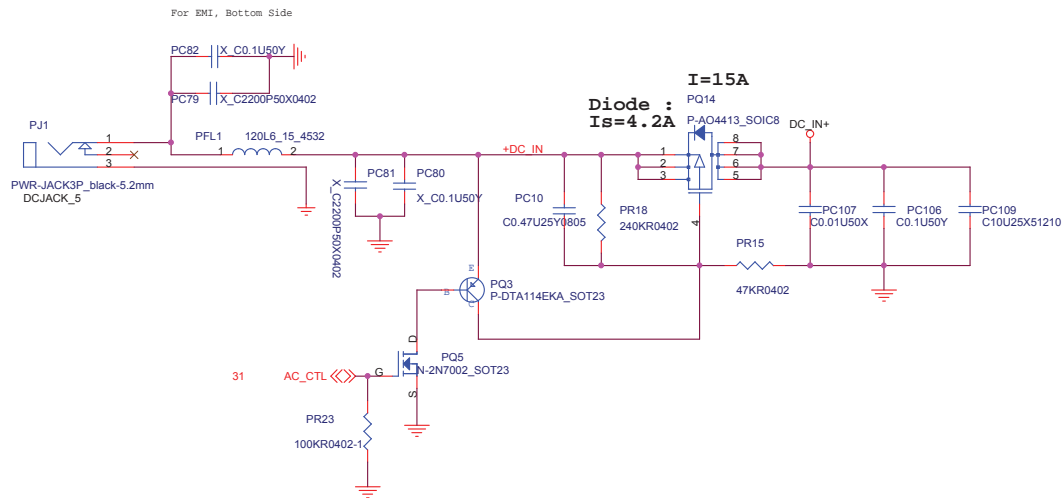


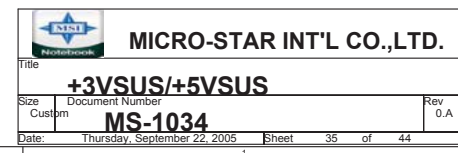


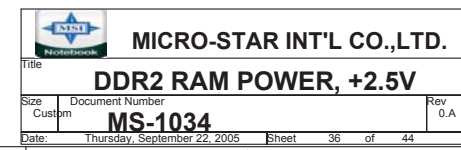
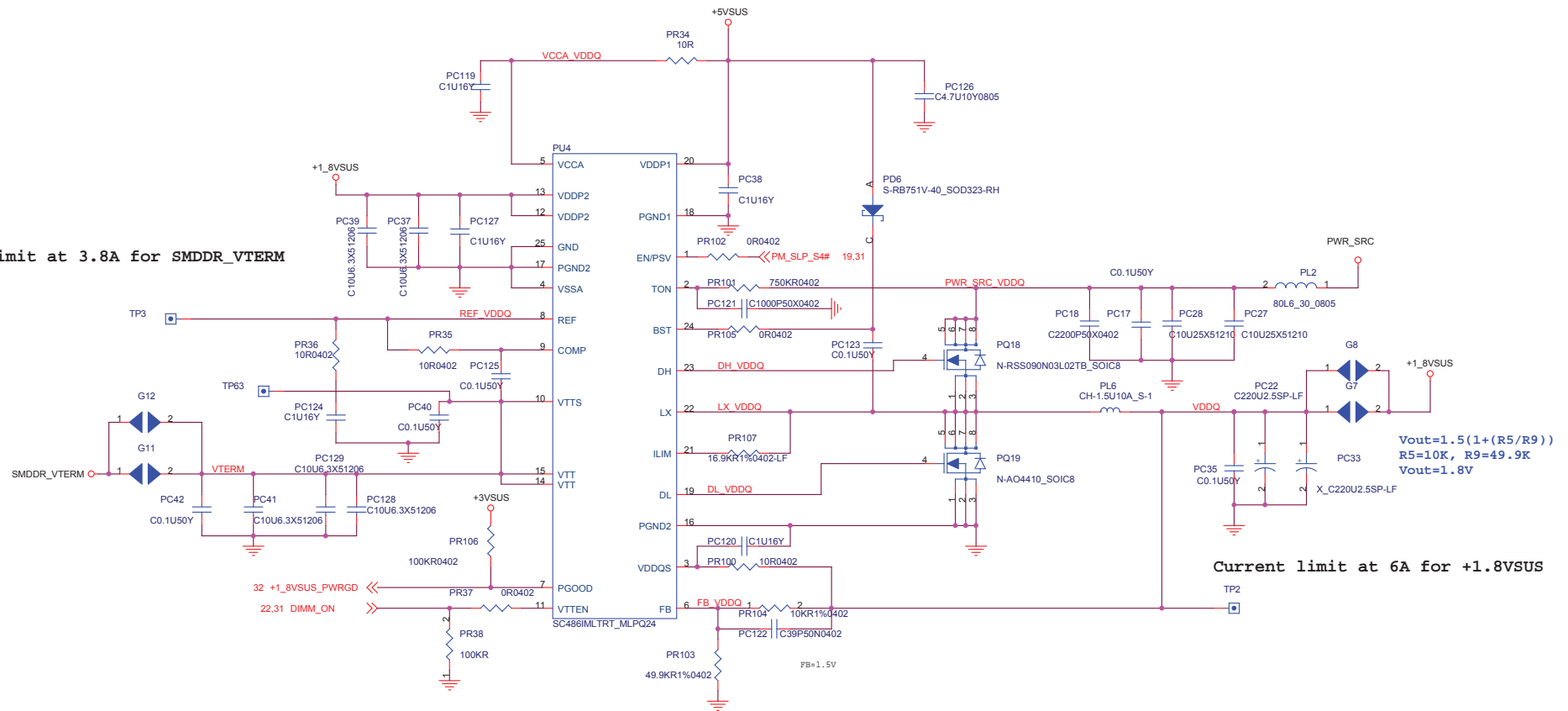
NO MSI P/N











The Limited Current = 10A

$$V_{out} = V_{ref} (105k) / (124k + 44.2k + 105k)$$

$$V_{ref} = 2.75V$$

$$V_{out} = 1.05V$$

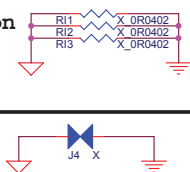
Current Limit at 6 Amp

$$V_{out} = V_{ref} (105k + 44.2k) / (124k + 44.2k + 105k)$$

$$V_{ref} = 2.75V$$

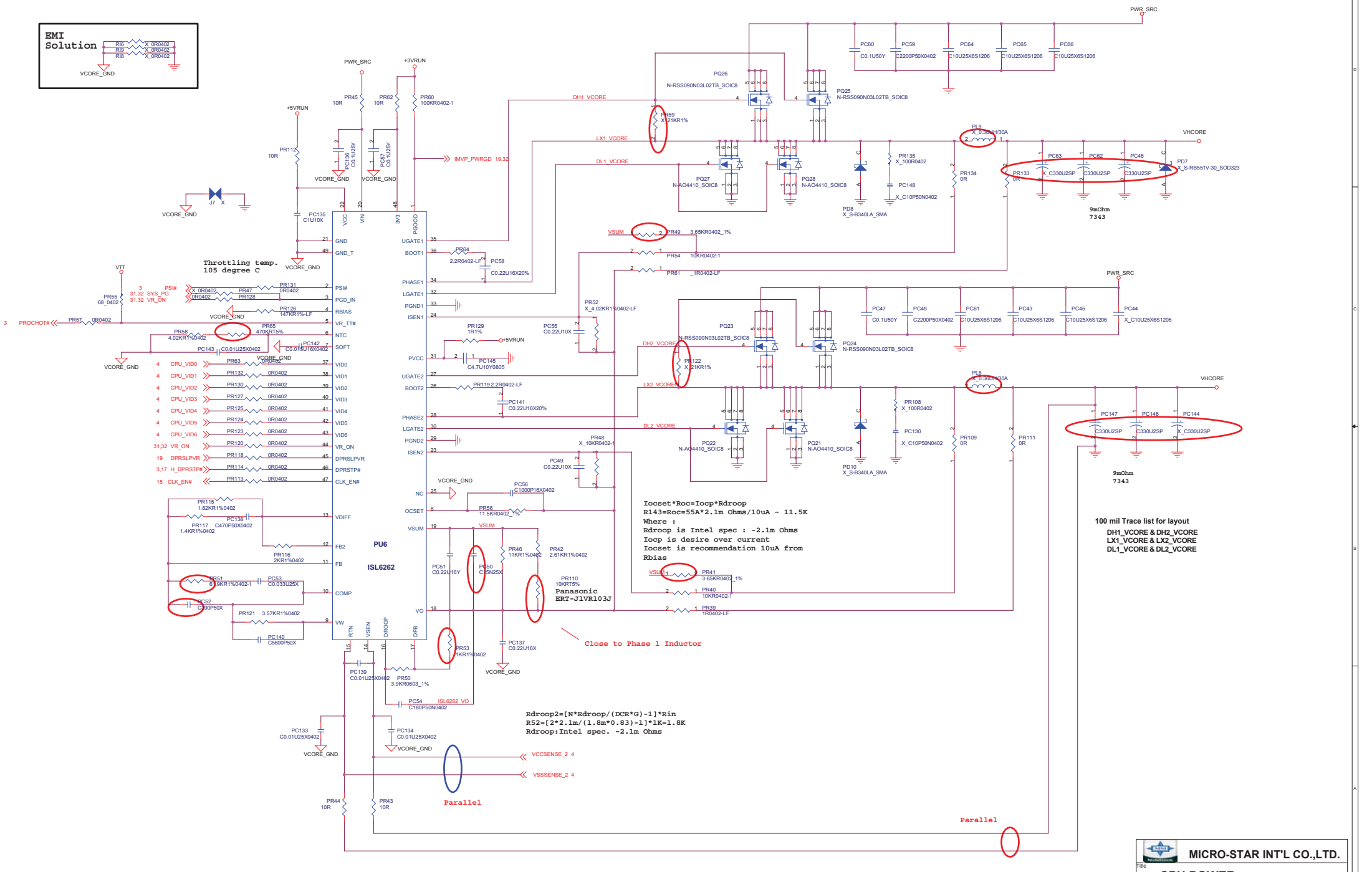
$$V_{out} = 1.50V$$

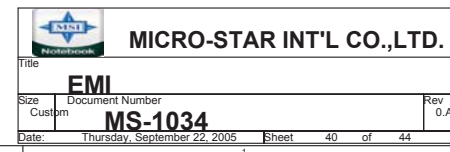
EMI
Solution



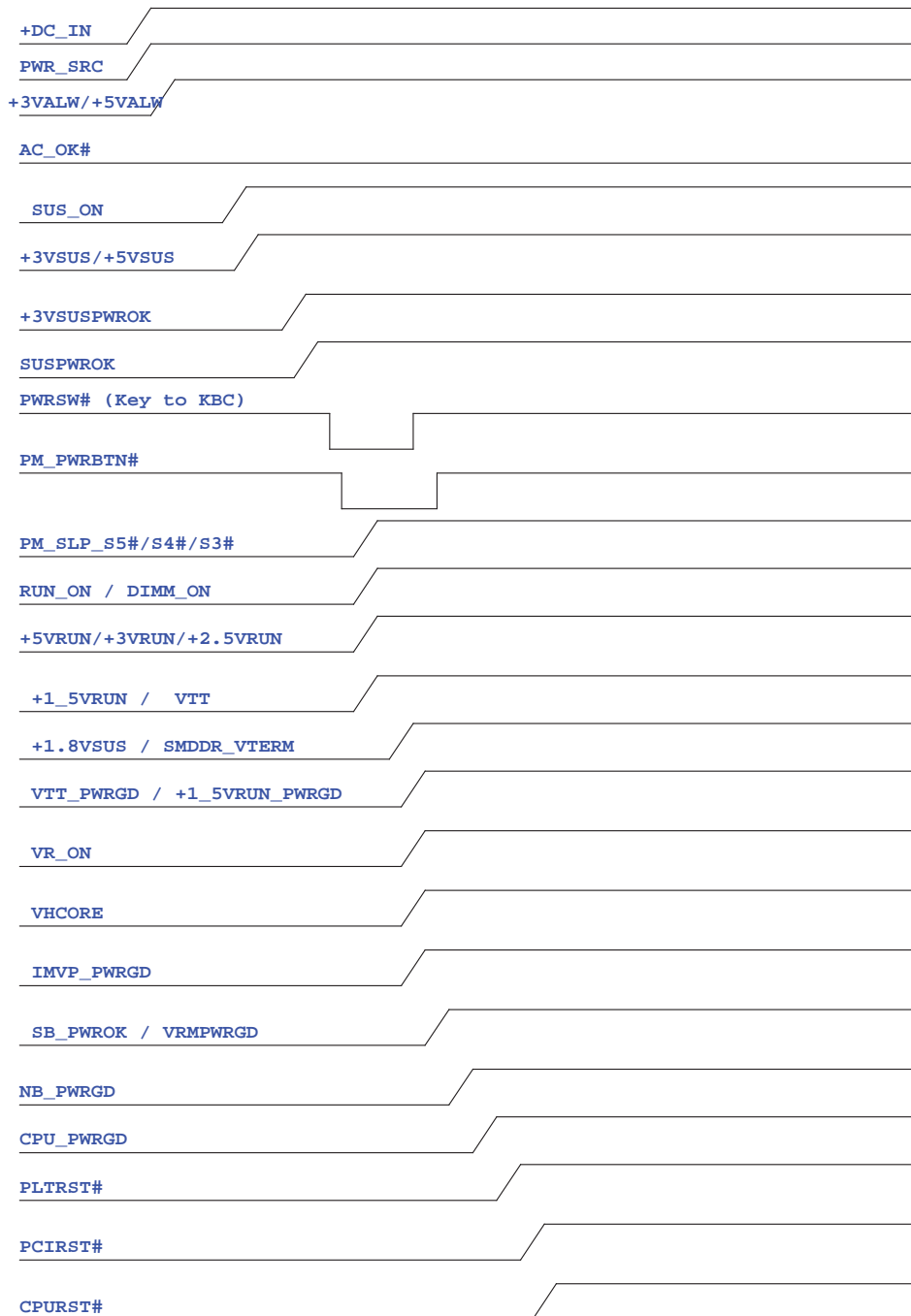
32 VTT_PWRGD << VTT_PWRGD

+1_5VRUN_PWRGD >> +1_5VRUN_PWRGD 32

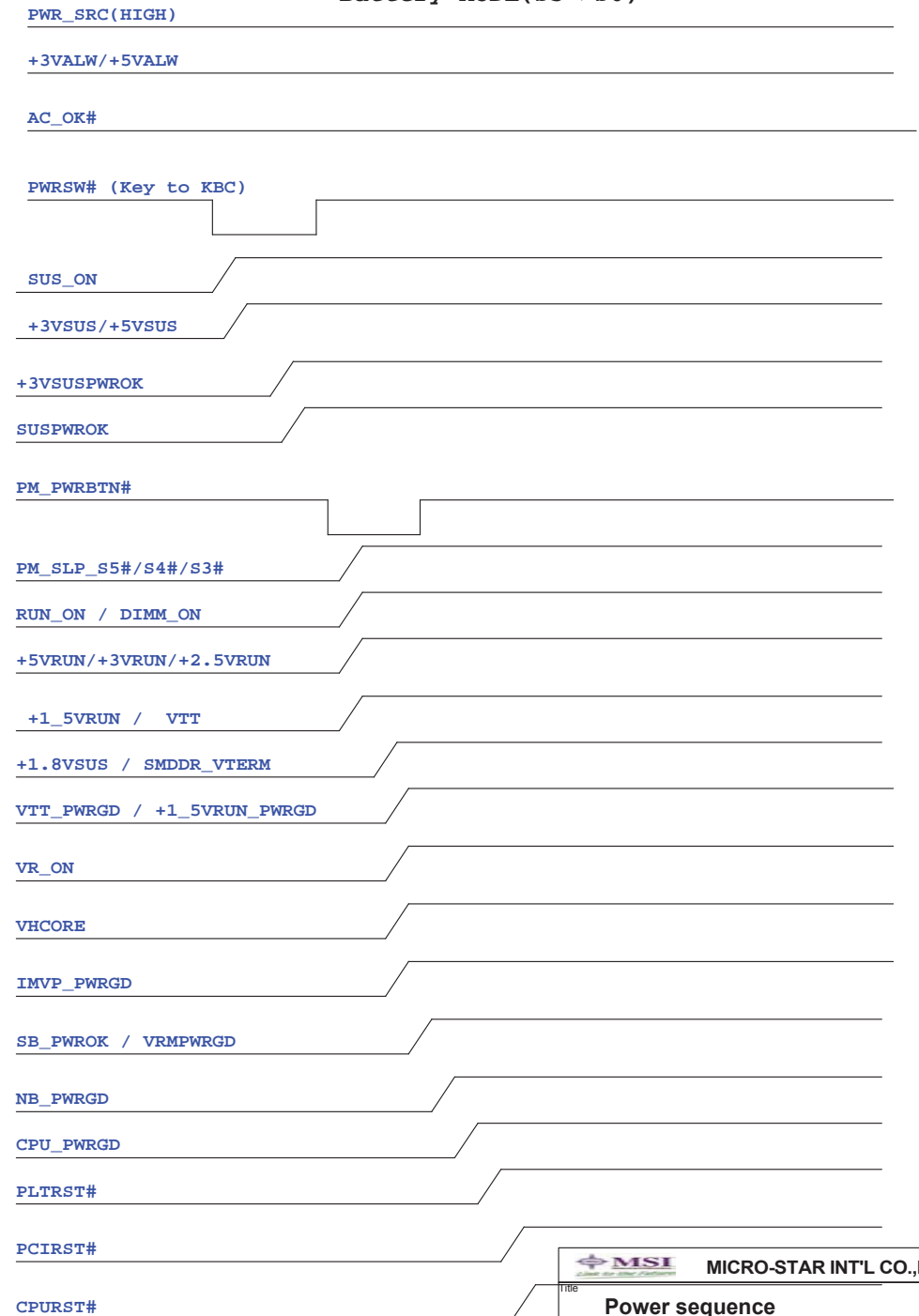




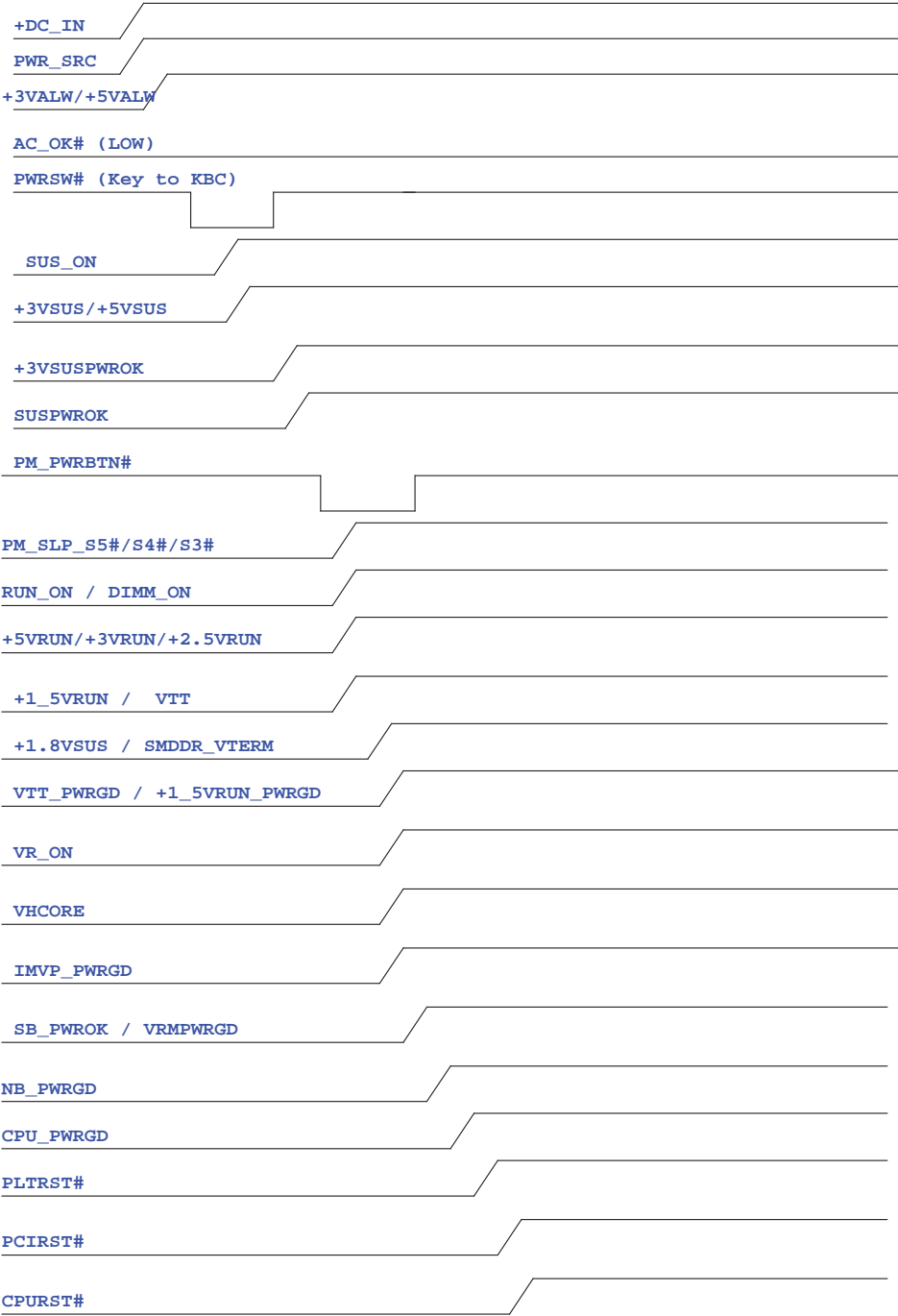
AC MODE(S5->S0)

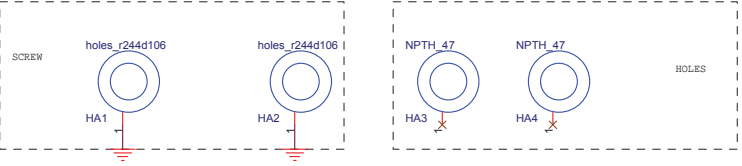
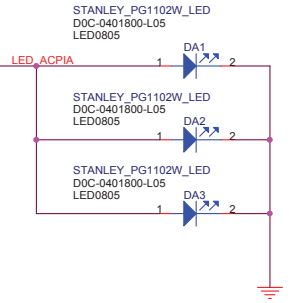
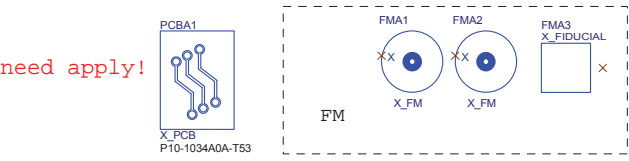
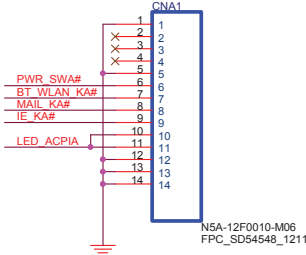
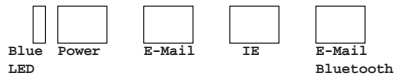
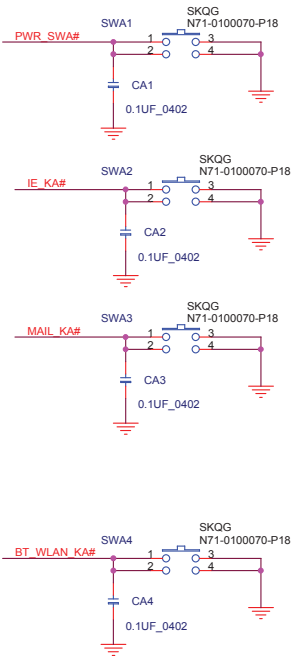
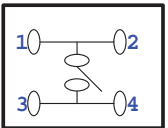


Battery MODE(S5->S0)

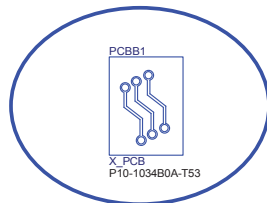
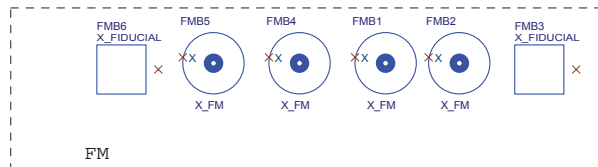
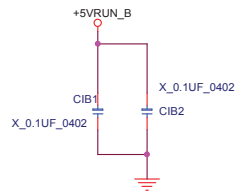
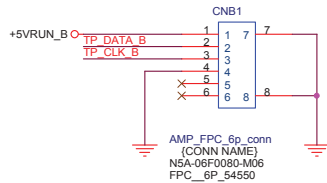
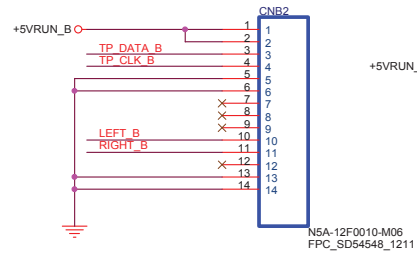
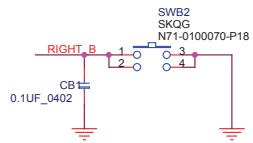
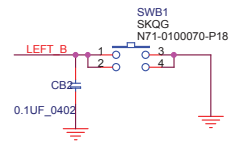


POWER UP (G3->S0)

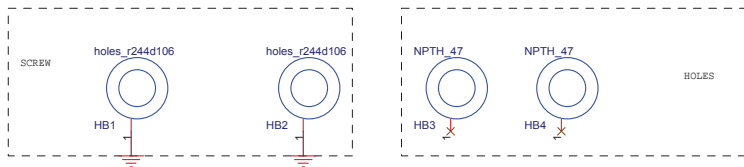




Title		
Launch Board for MS1034		
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Need to apply



Title			
TP Board			
Size	Document Number		Rev
Custom	MS-1034B		110
Date:	Thursday, September 22, 2005	Sheet	44 of 44